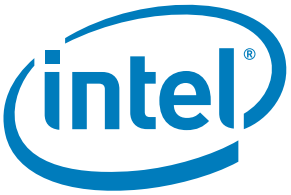

Intel® C610 Series Chipset and Intel® X99 Chipset Platform Controller Hub (PCH)

External Design Specification (EDS) Specification Update

June 2016

Reference Number: 330789-004

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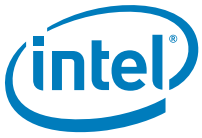

Contents

Revision History

CDI/IBL Document No	Revision	Description	Date
330789	001	• Initial Release	August 2014
330789	002	• Added Intel® C610 Series Chipset	September 2014
330789	003	• Added Errata 27xHCI reset may cause system hang • Updated SRTCRST VIH minimum value same as RTCRST value as 2.0 V	January 2016
330789	004	• Updated errata 25 : changed workaround to None	June 2016

§

Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Document Number
Intel® C610 Series Chipset and Intel® X99 Chipset Platform Controller Hub (PCH) Datasheet	330788

Nomenclature

Errata are design defects or errors. Errata may cause the behavior of the PCH to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present in all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

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Summary Tables of Changes

The following tables indicate the errata, specification changes, specification clarifications, or documentation changes which apply to the Product Name product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. These tables uses the following notations:

Codes Used in Summary Tables

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Plan Fix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.

Row

Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata (Sheet 1 of 2)

Erratum Number	Stepping			Status	ERRATA
	A0	B0	B1		
1	x	x	x	No Fix	Intel® Management Engine in PCH might send out MCTP messages with non-zero PAD bytes
2	x	x	x	No Fix	Reads from Flash Descriptor Region 5 and 6 using FDOC/FDOD Registers may respond to wrong addresses
3	x	x	x	No Fix	USB Isoch in Transfer Error Issue
4	x	x	x	No Fix	USB Babble Detected with SW Over-scheduling
5	x	x	x	No Fix	USB Low-Speed/Full-Speed EOP Issue
6	x	x	x	No Fix	Asynchronous Retries Prioritized Over Periodic Transfers
7	x	x	x	No Fix	USB FS/LS Incorrect Number of Retries
8	x	x	x	No Fix	USB Full-/Low- speed Port Reset or Clear TT Buffer Request
9	x	x	x	No Fix	xHC Data Packet Header and Payload Mismatch Error Condition
10	x	x	x	No Fix	USB SuperSpeed* Packet with Invalid Type Field Issue

Errata (Sheet 2 of 2)

Erratum Number	Stepping			Status	ERRATA
	A0	B0	B1		
11	x	x	x	No Fix	xHC Behavior with Three Consecutive Failed U3 Entry Attempts
12	x	x	x	No Fix	Incorrect IRQ (x) Vector Returned for 8259 Interrupts With RAEOI Enabled
13	x	x	x	No Fix	USB RMH Think Time Issue
14	x	x	x	No Fix	Max Packet Size and Transfer Descriptor Length Mismatch
15	x	x	x	No Fix	USB Full-/Low- speed Device Removal Issue
16	x	x	x	No Fix	Intel ME ROM will not boot if ME FW region crosses 16 MB boundary in SPI Flash
17	x	x	x	No Fix	PCI-Express Root Ports Unsupported Request Completion Issue
18	x	x	x	No Fix	SuperSpeed Device Tree Hot Plug Issue
19	x	x	x	No Fix	xHC Endpoint Count Issue
20	x	x	x	No Fix	Electrical Fast Transient Burst Test Issue
21	x	x	x	No Fix	PCIe* Tx rise/fall mismatch fails PCIe Gen2 spec
22	x	x	x	No Fix	SATA and sSATA Signal Voltage Level Violation
23	x	x	x	No Fix	Set Latency Tolerance Value Command Completion Event Issue
24	x	x	x	No Fix	RMH Port Disabled Due to Device Initiated Remote Wake
25	x	x	x	No Fix	XHCI Controller May Delay Transactions Due to Short Packets Issue
26	x	x	x	No Fix	System may hang with concurrent read transaction to the Server Platform Service Rom (SPSR) function and configuration transaction to the MS SMBus controllers
27	x	x	x	No Fix	xHCI reset may cause system hang

Specification Changes

Spec Change Number	Stepping			SPECIFICATION CHANGES
	A0	B0	B1	

Specification Clarification

No.	Document Revision	SPECIFICATION CLARIFICATIONS

Documentation Changes

No.	Document Revision	DOCUMENTATION CHANGES

Identification Information

Markings

SKU	Phase	PCH Stepping	S-Spec	QDF	MM#	ROHS Compliant	Notes
Intel® C612 Chipset	Production	B1	SLKM8	N/A	938954	Yes	Intel® C612 Chipset (Intel®DH82029 PCH)
Intel®X99 Chipset	Production	B1	SLKM9	N/A	938955	Yes	Intel®X99 Chipset (Intel® DHX99 PCH)

Intel® C610 Series Chipset and Intel® X99 Chipset Device and Revision Identification

Device Function	Description	Dev ID	A0 Rev ID	B0 Rev ID	B1 Rev ID	Comments
D31:F0	LPC	8D40h	02h	04h	05h	Preproduction
		8D44h	02h	04h	05h	Wellsburg-G
		8D47h	02h	04h	05h	Wellsburg-X
D31:F2	SATA	8D00h	02h	04h	05h	Non-AHCI and Non-RAID Mode
		8D02h	02h	04h	05h	AHCI (Ports 0-5)
		2822h	02h	04h	05h	RAID 0/1/5/10 if AIE (D31:F2 Offset 9Ch bit 7) = 0 and AIES (D31:F2 Offset 9Ch bit 6) = 0.
		8D06h	02h	04h	05h	Premium RAID 0/1/5/10 if AIE (D31:F2 Offset 9Ch bit 7) = 1.
		2826h	02h	04h	05h	Premium RAID 0/1/5/10 if AIE (D31:F2 Offset 9Ch bit 7) = 0 and AIES (D31:F2 Offset 9Ch bit 6) = 1.
D31:F5	SATA	8D08h	02h	04h	05h	Non AHCI and Non RAID (ports 4 and 5)
D17:F4	sSATA	8D60h	02h	04h	05h	Non-AHCI and Non-RAID mode
		8D62h	02h	04h	05h	AHCI mode
		8D66h	02h	04h	05h	Premium RAID 0/1/5/10
		2823h	02h	04h	05h	RAID 0/1/5/10 if AIE (D17:F4 Offset 9Ch bit 7) = 0 and AIES (D17:F4 Offset 9Ch bit 6) = 0.
		2827h	02h	04h	05h	Premium RAID 0/1/5/10 if AIE (D17:F4 Offset 9Ch bit 7) = 0 and AIES (D17:F4 Offset 9Ch bit 6) = 1.
D31:F3	SMBus	8D22h	02h	04h	05h	SMBus
D31:F6	Thermal	8D24h	02h	04h	05h	Thermal
D29:F0 or D29:F7	USB EHCI #1	8D26h	02h	04h	05h	EHCI Controller #1
D26:F0 or D26:F7	USB EHCI #2	8D2Dh	02h	04h	05h	EHCI Controller #2
D20:F0	USB xHCI	8D31h	02h	04h	05h	xHCI Controller
D27:F0	Intel HD Audio	8D20 or 8D21h	02h	04h	05h	Intel High Definition Audio
D28:F0	PCI Express Port 1	8D10h or 8D11h	D2h	D4h	D5h	When D28:F0:ECh:bit 1= 0
		244Eh	D2h	D4h	D5h	When D28:F0:ECh:bit 1= 1

Device Function	Description	Dev ID	A0 Rev ID	B0 Rev ID	B1 Rev ID	Comments
D28:F1	PCI Express Port 2	8D12h or 8D13h	D2h	D4h	D5h	When D28:F1:ECh:bit 1 = 0
		244Eh	D2h	D4h	D5h	When D28:F1:ECh:bit 1 = 1
D28:F2	PCI Express Port 3	8D14h or 8D15h	D2h	D4h	D5h	When D28:F2:ECh:bit 1 = 0
		244Eh	D2h	D4h	D5h	When D28:F2:ECh:bit 1 = 1

Device Function	Description	Dev ID	A0 Rev ID	B0 Rev ID	B1 Rev ID	Comments
D28:F3	PCI Express Port 4	8D16h or 8D17h	D2h	D4h	D5h	When D28:F3:ECh:bit 1 = 0
		244Eh	D2h	D4h	D5h	When D28:F3:ECh:bit 1 = 1
D28:F4	PCI Express Port 5	8D18h or 8D19h	D2h	D4h	D5h	When D28:F4:ECh:bit 1 = 0
		244Eh	D2h	D4h	D5h	When D28:F4:ECh:bit 1 = 1
D28:F5	PCI Express Port 6	8D1A or 8D1Bh	D2h	D4h	D5h	When D28:F5:ECh:bit 1 = 0
		244Eh	D2h	D4h	D5h	When D28:F5:ECh:bit 1 = 1
D28:F6	PCI Express Port 7	8D1Ch or 8D1Dh	D2h	D4h	D5h	When D28:F6:ECh:bit 1 = 0
		244Eh	D2h	D4h	D5h	When D28:F6:ECh:bit 1 = 1
D28:F7	PCI Express Port 8	8D1Eh or 8D1Fh	D2h	D4h	D5h	When D28:F7:ECh:bit 1 = 0
		244Eh	D2h	D4h	D5h	When D28:F7:ECh:bit 1 = 1
D25:F0	LAN	8D33h	02h	04h	05h	LAN
D22:F0	MEI #1	8D3Ah	02h	04h	05h	Intel ME Interface #1 - HECI#1
D22:F1	MEI #2	8D3Bh	02h	04h	05h	Intel ME Interface #2 - HECI#2
D22:F2	IDE-R	8D3Ch	02h	04h	05h	IDE-R
D22:F3	KT	8D3Dh	02h	04h	05h	KT
D17:F0	SPSR	8D7Ch	02h	04h	05h	MS Unit
D17:F1	MS SMBus0	8D7Dh	02h	04h	05h	MS Unit
D17:F2	MS SMBus1	8D7Eh	02h	04h	05h	MS Unit
D17:F3	MS SMBus2	8D7Fh	02h	04h	05h	MS Unit

Intel® C610 Series Chipset and Intel® X99 Chipset CRID Table

CRID Select Keys	PCH Stepping	Rev ID	CRID Value	Notes
1Dh	A0	02h	02h	Enable CRID by writing 1Dh to D31:F0:Offset 08h
	B0	04h	04h	
	B1	05h	05h	

The RID register will not retain its value during suspend states. To prevent undesirable enumeration events, the system BIOS must re-select the CRID during resume events from ACPI S3 or S4 states.

Errata

1. Intel® Management Engine in PCH might send out MCTP messages with non-zero PAD bytes

Problem: The Intel® Management Engine (Intel® ME) in PCH might send out MCTP messages with PAD bytes not equal to 0x00, which violates the definition of PAD bytes in Management Component Transport Protocol (MCTP) PCIe VDM Transport Binding Specification, version 1.0.1.

Implication: As defined in above MCTP spec, PAD bytes are bytes of 0x00 as required to fill out the overall PCIe VDM data to make sure it's dword aligned. PAD bytes do not contain valid information, so no functional issues or data loss/corruption will be caused by the violation stated above.

Workaround: None

Status: No plan to Fix

2. Reads from Flash Descriptor Region 5 and 6 using FDOC/FDOD Registers may respond to wrong addresses

Problem: Reads of the Region Base and Limit information for SPI Flash Descriptor Region 5 (Device Expansion) and Region 6 (Secondary BIOS) using the Flash Descriptor Observability Control (FDOC) and Flash Descriptor Observability Data (FDOD) registers will respond to wrong address offsets instead of the spec-defined ones. Flash Descriptor Region 5 responds to address offset 0x20h instead of 0x14h as defined in 4.1.3.6 of Wellsburg SPI Programming Guide, Rev1.0 Flash Descriptor Region 6 responds to address offset 0x40h instead of 0x18h as defined in 4.1.3.7 of Wellsburg SPI Programming Guide, Rev1.0.

Implication: Reads of the Region Base and Region Limit information for SPI Flash Descriptor Region 5 and Region 6 using the FDOC and FDOD registers with the spec-defined address offsets will not return correct data. Reads via other methods are not impacted.

Workaround: If reading the Region Base and Region Limit information using FDOC and FDOD registers, use offset 0x20h for Flash Descriptor Region 5 and 0x40h for Flash Descriptor Region 6.

Status: No plan to Fix

3. USB Isoch in Transfer Error Issue

Problem: If a USB full-speed inbound isochronous transaction with a packet length 190 bytes or greater is started near the end of a microframe, the PCH may see more than 189 bytes in the next microframe. If the PCH sees more than 189 bytes for a microframe an error will be sent to software and the isochronous transfer will be lost. If a single data packet is lost not perceptible impact for the end user is expected.

Implication: If the PCH sees more than 189 bytes for a microframe an error will be sent to software and the isochronous transfer will be lost. If a single data packet is lost no perceptible impact for the end user is expected.

Workaround: None

Status: No plan to Fix

4. USB Babble Detected with SW Over-scheduling

Problem: If software violates USB periodic scheduling rules for full-speed isochronous traffic by over-scheduling, the RMH may not handle the error condition properly and return a completion split with more data than the length expected.

Implication: If the RMH returns more data than expected, the endpoint will detect packet babble for that transaction and the packet will be dropped. Since over-scheduling occurred to create the error condition, the packet would be dropped regardless of RMH behavior. If

a single isochronous data packet is lost, no perceptible impact to the end user is expected.

Workaround: None

Status: No plan to Fix

5. USB Low-Speed/Full-Speed EOP Issue

Problem: If the EOP of the last packet in a USB Isochronous split transaction (Transaction >189 bytes) is dropped or delayed 3 ms or longer the following may occur:

- If there are no other pending low-speed or full-speed transactions the RMH will not send SOF, or Keep-Alive. Devices connected to the RMH will interpret this condition as idle and will enter suspend.
- If there is other pending low-speed or full-speed transactions, the RMH will drop the isochronous transaction and resume normal operation.
- If there are no other transactions pending, the RMH is unaware a device entered suspend and may starting sending a transaction without waking the device. The implication is device dependent, but a device may stall and require a reset to resume functionality.
- If there are other transactions present, only the initial isochronous transaction may be lost. The loss of a single isochronous transaction may not result in end user perceptible impact.

Implication: None

Workaround: No plan to fix

6. Asynchronous Retries Prioritized Over Periodic Transfers

Problem: The integrated USB RMH incorrectly prioritizes full-speed and low-speed asynchronous retries over dispatchable periodic transfers.

Implication: Periodic transfers may be delayed or aborted. If the asynchronous retry latency causes the periodic transfer to be aborted, the impact varies depending on the nature of periodic transfer:

- If a periodic interrupt transfer is aborted, the data may be recovered by the next instance of the interrupt or the data could be dropped.
- If a periodic isochronous transfer is aborted, the data will be dropped. A single dropped periodic transaction should not be noticeable by end user.

Workaround: None

Status: No plan to fix

7. USB FS/LS Incorrect Number of Retries

Problem: A USB low-speed transaction may be retried more than three times, and a USB fullspeed transaction may be retried less than three times if all of the following conditions are met:

- A USB low-speed transaction with errors, or the first retry of the transaction occurs near the end of a microframe, and there is not enough time to complete another retry of the low-speed transaction in the same microframe.
- There is pending USB full-speed traffic and there is enough time left in the microframe to complete one or more attempts of the full-speed transaction.
- Both the low-speed and full-speed transactions must be asynchronous (Bulk/ Control) and must have the same direction either in or out.

Implication:

- For low-speed transactions the extra retry(s) allow a transaction additional chance(s) to recover regardless of if the full-speed transaction has errors or not.

- If the full-speed transactions also have errors, the PCH may retry the transaction fewer times than required, stalling the device prematurely. Once stalled, the implication is software dependent, but the device may be reset by software.

Workaround: None

Status: No plan to Fix

8. USB Full-/Low- speed Port Reset or Clear TT Buffer Request

Problem: One or more full-/low-speed USB devices on the same RMH controller may be affected if the devices are not suspended and either (a) software issues a Port Reset OR (b) software issues a Clear TT Buffer request to a port executing a split full-/low-speed Asynchronous Out command.

- The small window of exposure for full-speed device is around 1.5 microseconds and around 12 microseconds for a low-speed device.

Implication: The affected port may stall or receive stale data for a newly arrived split transfer occurring at the time of the Port Reset or Clear TT Buffer request.

Workaround: None

Status: No plan to Fix

9. xHC Data Packet Header and Payload Mismatch Error Condition

Problem: If a SuperSpeed device sends a Data Packet Header (DPH) to the xHC with a data length field that specifies less data than is actually sent in the Data Packet Payload (DPP), the xHC will accept the packet instead of discarding the packet as invalid.

Note: The USB 3.0 specification requires a device to send a DPP matching the amount of data specified by the DPH.

Implication: The amount of data specified in the DPH will be accepted by the xHC and the remaining data will be discarded and may result in anomalous system behavior.

Note: This issue has only been observed in a synthetic test environment with a synthetic device.

Workaround: None

Status: No plan to Fix

10. USB SuperSpeed* Packet with Invalid Type Field Issue

Problem: If the encoding for the “type” field for a SuperSpeed packet is set to a reserved value and the encoding for the “subtype” field is set to “ACK”, the xHC may accept the packet as a valid acknowledgment transaction packet instead of ignoring the packet.

Implication: System implication is dependent on the misbehaving device and may result in anomalous system behavior.

Workaround: None

Status: No plan to Fix

11. xHC Behavior with Three Consecutive Failed U3 Entry Attempts

Problem: The xHC does not transition to the SS.Inactive USB 3.0 LTSSM (Link Training and Status State Machine) state after a SuperSpeed device fails to enter U3 upon three consecutive attempts.

Implication: The xHC will continue to try to initiate U3. The implication is driver and operating system dependent.

Workaround: None

Status: No plan to Fix

12. Incorrect IRQ (x) Vector Returned for 8259 Interrupts With RAEOI Enabled

Problem: If multiple interrupts are active prior to an interrupt acknowledge cycle with Rotating Automatic End of Interrupt (RAEOI) mode of operation enabled for 8259 interrupts (0-7), an incorrect IRQ(x) vector may be returned to the processor.

Implication: Implications of an incorrect IRQ(x) vector being returned to the CPU are SW implementation dependent.

Workaround: None

Status: No plan to Fix

13. USB RMH Think Time Issue

Problem: The USB RMH Think Time may exceed its declared value in the RMH hub descriptor register of 8 full-speed bit times.

Implication: If the USB driver fully subscribes a USB microframe, LS/FS transactions may exceed the microframe boundary.

Workaround: None

Status: No plan to Fix

14. Max Packet Size and Transfer Descriptor Length Mismatch

Problem: The xHC may incorrectly handle a request from a low-speed or full-speed device when all the following conditions are true:

- The sum of the packet fragments equals the length specified by the Transfer Descriptor (TD)
- The TD length is less than the MPS (Max Packet Size) for the device
- The last packet received in the transfer is “0” or babble bytes

Implication: The xHC will halt the endpoint if all the above conditions are met. All functions associated with the endpoint will stop functioning until the device is unplugged and reinserted.

Workaround: None

Status: No plan to Fix

15. USB Full-/Low- speed Device Removal Issue

Problem: If two or more USB full-/low-speed devices are connected to the same USB controller, the devices are not suspended, and one device is removed, one or more of the devices remaining in the system may be affected by the disconnect.

Implication: The implication is device dependent. A device may experience a delayed transaction, stall and be recovered via software, or stall and require a reset such as a hot plug to resume normal functionality.

Workaround: None

Status: No plan to Fix

16. Intel ME ROM will not boot if Intel ME FW region crosses 16 MB boundary in SPI Flash

Problem: If the Intel ME FW region crosses the 16 MB boundary in SPI flash, Intel ME will not boot.

Implication: Board might not power up due to Intel ME not booting.

Workaround: Be sure Intel ME FW image completely fits into the lower 16 MB region of the SPI flash.

Status: No plan to Fix

17. PCI-Express Root Ports Unsupported Request Completion Issue

Problem: The PCIe* root ports may return an Unsupported Request (UR) completion with an incorrect lower address field in response to a memory read if any of the following occur:

- BIOS disables Bus Master Enable in the PCIe Root Port's Command register (PCICMD bit 2 =0)
- A non-zero Address Type (AT) field of the Transaction Layer Packet (TLP) header
- The requested upstream address falls within the memory range claimed by the secondary side of the bridge
- Requester ID with Bus Number of 0

Implication: The UR Completion with an incorrect lower address field may be handled as a Malformed TLP causing the Requestor to send a ERR_NONFATAL or ERR_FATAL message upstream to the root port.

Workaround: None.

Status: No plan to Fix

18. SuperSpeed Device Tree Hot Plug Issue

Problem: If there are two outstanding USB split transactions on a device tree with more than one Full-Speed or Low-Speed periodic endpoint behind an external High-Speed hub and the device tree is unplugged, the xHC may fail to properly flush the outstanding split transactions.

Implication: If a device tree with more than one Full-Speed or Low-Speed periodic endpoint behind an external High-Speed hub is inserted into an xHC port, the system may hang.

Workaround: Set xHCI MMIO + 0x8094[14] to 1b and xHCI MMIO + 0x8094[21] to 1b.

Status: No plan to Fix

19. xHC Endpoint Count Issue

Problem: All USB devices contain a bidirectional control endpoint. The xHC counts each control endpoint as two separate endpoints, one for each direction.

Implication: The implication is USB driver specific. The Intel USB driver counts each control endpoint as a single endpoint causing discrepancy with hardware endpoint counts. The Intel USB driver may try to subscribe more endpoints than the xHC hardware can support which may result in anomalous device behavior.

Workaround: Clear xHCI MMIO+0x805C[22] to 0b

Status: No plan to Fix

20. Electrical Fast Transient Burst Test Issue

Problem: Failures may be observed when testing for the International Electromechanical Commission's (IEC) electrical fast transient / burst immunity standard on the USB 2.0 interface.

Note: The electrical fast transient / burst immunity test is defined by the IEC 61000-4-4 standard. IEC standard 60601-1-2 requires medical equipment and systems to pass test level 3 of the IEC 61000-4-4 standard.

Implication: During electrical fast transient / burst immunity testing at +/- 1000 V, USB 2.0 devices may be dropped, the system may hang, or other undesired behavior may occur.

Note: The voltage test level varies based on intended platform use.

Workaround: None

Status: No plan to Fix

21. PCIe* Tx rise/fall mismatch fails PCIe Gen2 spec

Problem: PCH PCIe* transmitters may violate the Gen 2 (5 GT/s) rise/fall mismatch specification defined in section 4.3.3.5 of PCI Express® Base Specification, Rev 2.1.

Implication: No system performance or functional failures have been observed as a result of this violation.

Workaround: None

Status: No plan to Fix

22. SATA and sSATA Signal Voltage Level Violation

Problem: SATA and sSATA transmit buffers have been designed to maximize performance and robustness over a variety of routing scenarios. As a result, SATA and sSATA transmit signaling voltage levels may exceed the maximum motherboard TX connector and device RX connector voltage specifications as defined in section 7.2.2.3 of the Serial ATA specification, rev 3.1. This issue applies to Gen 1 (1.5 Gb/s) and Gen 2 (3.0 Gb/s).

Implication: None known

Workaround: None

Status: No plan to Fix

23. Set Latency Tolerance Value Command Completion Event Issue

Problem: The xHCI controller does not return a value of '0' for slot ID in the command completion event TRB (Transfer Request Block) for a set latency tolerance value command.

Note: This violates the command completion event TRB description in section 6.4.2.2 of the eXtensible Host Controller Interface for Universal Serial Bus (xHCI) specification, revision 1.0.

Implication: There are no known functional failures due to this issue.

Note: Set latency tolerance value command is specific to the controller and not the slot. Software knows which command was issued and which fields are valid to check for the event.

Note: xHCI CV compliance test suite: Test TD4.10: Set Latency Tolerance Value Command Test may issue a warning. No wavier from USBIF required for this warning.

Workaround: None

Status: No plan to Fix

24. RMH Port Disabled Due to Device Initiated Remote Wake

Problem: During resume from Global Suspend, the RMH controller may not send SOF soon enough to prevent a device from entering suspend again. A collision on the port may occur if a device initiated remote wake occurs before the RMH controller sends SOF.

Note: Intel has only observed this issue when two USB devices on the same RMH controller send remote wake within 30ms window while RMH controller is resuming from Global Suspend.

Implication: The RMH host controller may detect the collision as babble and disable the port.

Workaround: Intel recommends system software to check bit 3 (Port Enable/Disable Change) together with bit 7 (Suspend) of Port N Status and Control PORTC registers when determining which port(s) have initiated remote wake.

Status: No plan to Fix

25. XHCI Controller May Delay Transactions Due to Short Packets Issue

Problem: If the software driver for a USB 3.0 bulk device continuously schedules large Transfer Descriptors (TDs) and the device frequently responds with a short packet (defined in the USB specification), the xHCI Host controller may delay service to other device's endpoints.

Implication: The implication is device dependent.

- Full Speed and Low Speed devices with Interrupt IN endpoints connected to the XHCI controller behind a USB hub may experience split transaction errors causing the USB hub and USB devices behind the hub to be re-enumerated.
- Isochronous devices connected to the XHCI controller may experience dropped packets. Dropped audio or video packets may or may not result in end user detectable impact.

Note: Intel has only observed these implications with high resolution USB 3.0 Cameras that use bulk transfers to continuously send TDs of approximately 1 MB or greater.

Workaround: None

Status: No plan to Fix

26. System may hang with concurrent read transaction to the Server Platform Service Rom (SPSR) function and configuration transaction to the MS SMBus controllers

Problem: If the MS SMBus is configured as host-controlled, and enabled along with the SPSR function, and if there is concurrent configuration transaction to the MS SMBus and read transaction to SPSR, a conflict may occur between the two transactions if the completions to both transactions arrive at the same time.

Implication: System may hang if above exact scenario is hit.

Note: Intel has only reproduced the issue in simulation environment, but not with real silicon. As today Intel is not aware of any real usage model that can hit the exact scenario to trigger the issue.

Workaround: None

Status: No plan to Fix

27. xHCI Host Controller Reset May Cause a System Hang

Problem: xHCI Host Controller may not respond following system software setting (Bit 1 = '1') the Host Controller Reset (HCRST) of the USB Command Register (xHCIBAR + 80h).

Implication: CATERR may occur resulting in a system hang.

Workaround: A 1ms delay is necessary anytime following System Software setting (Bit 1 = '1') Host Controller Reset (HCRST) of the USB Command Register (xHCIBAR + 80h).

Status: No plan to Fix

Specification Changes

There is no specification change in this revision.

Specification Clarification

There is no specification clarification in this revision.

Documentation Changes

There is no document change in this revision.

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