



DELTA-L+ FOR ELECTRICAL CHARACTERIZATION

Intel Corporation
Data Center Platform Application Engineering
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Purpose

- Material characterization is a critical step in PCB ecosystem enabling
 - Need to have a robust yet accurate method for the industry
 - Available industry methods have limitations in efficiency and accuracy
- Delta-L+ can provide:
 - accurate de-embedding with full S parameter extraction
 - material extraction capability
 - allow for flexibility/capability of HVM Monitoring by smaller coupon

PCB Characterization Process

Accurate Characterization /Material Selection

Material Selection



Production Board Samples



High Volume Manufacture Production

Intel (requirement)

Testing House

ODM/OEM

Material Vendor

PCB Manufacturer

ODM/OEM

PCB Manufacturer

Testing House

PCB Manufacturer

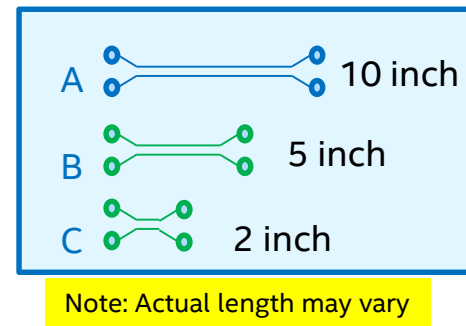
Quality Control

What's New in Delta-L+ compared to Delta-L 2.0?

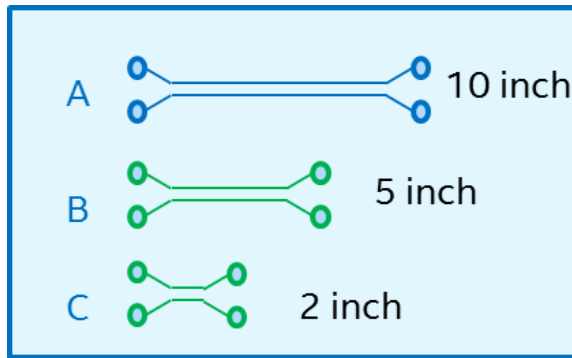
- Three-category approach to address the need of PCB characterization at different stages
- Major enhancements from Delta-L 2.0:
 - Three-length (3L) method to self-check and ensure the accuracy of the de-embedding results
 - One-length (1L) method for HVM monitoring
- Future enhancements (Working In Progress):
 - Dk/Df extraction methodology
 - Surface roughness characterization methodology

Delta-L+ Metrology

Choose coupons with different length combinations at different stages of PCB Characterization



3L



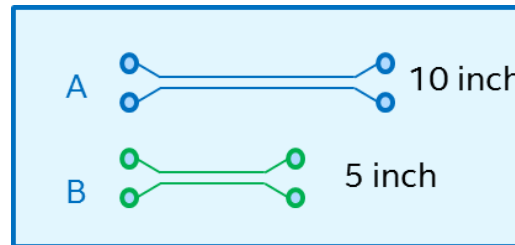
Best accuracy

Most suitable for:
Material Characterization
DK/DF Extraction, Insertion Loss &
Surface Roughness characterization

Typically <5 Boards

Material Selection

2L



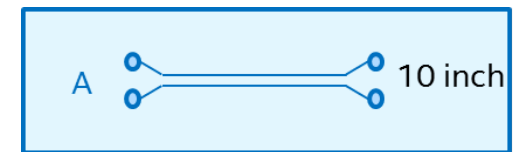
Cost effective

Most suitable for:
Board Quality Validation
Insertion loss & Impedance
validation

Typically 5-30 Boards

Board Sampling

1L



Small Coupon

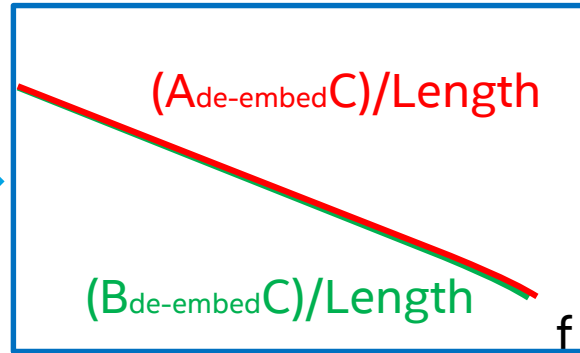
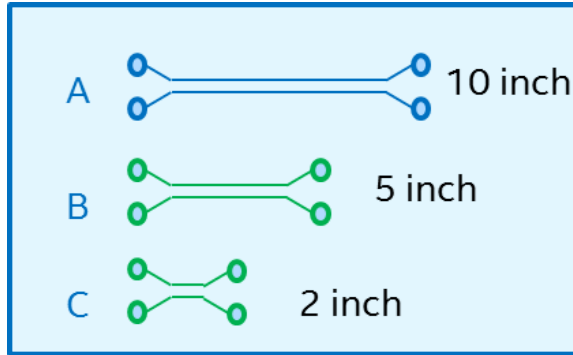
Most suitable for:
HVM Monitoring
Insertion loss and impedance
variation, by one-length approach

Sample size varies

HVM Monitoring

Delta-L+ (3L)

Three-Line Method



Dk/DF Extraction
SR Characterization

3L method

1. A de-embedded by C using 2X-thru de-embedding
2. B de-embedded by C using 2X-thru de-embedding
3. dB/in comparison of (A-C) and (B-C)
4. Dk/Df extraction

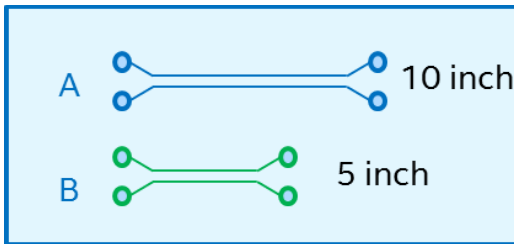
Note: Other de-embedding method, such as TRL, can be implemented as well

This is an important step to validate the de-embedded results.

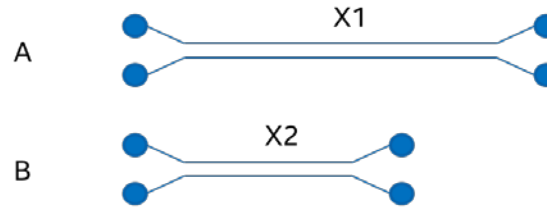
Criteria: < 5% (TBD) error @ up to the highest frequency of interest

Delta-L+ (2L)

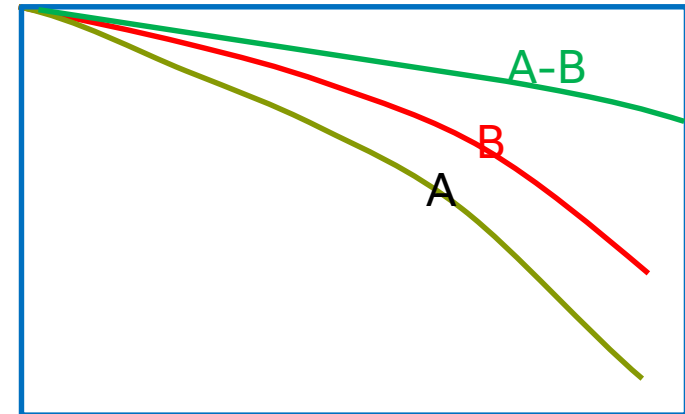
Two-Line Method Delta-L Methodology



Category 2 (two-line)
Direct A – B subtraction using Delta-L 2.0



- Direct through measurement for insertion loss.
 - Insertion of structure A: IL(A) -- X1 inches + vias
 - Insertion of structure B: IL(B) -- X2 inches + vias
 - $\text{dB/inch loss} = (\text{IL(A)} - \text{IL(B)}) / (X1 - X2)$
 - X2 cannot be too short, and X1-X2 better to be bigger than 3~4".
 - **Recommendation:** The routing length of X1 is twice of X2
- No full SOLT or TRL calibration needed; compatible to TRL calibration or AFR.
- VNA or TDR/TDT measurement
 - If TDT/TDT measured is performed, it needs to be converted to S parameter first.



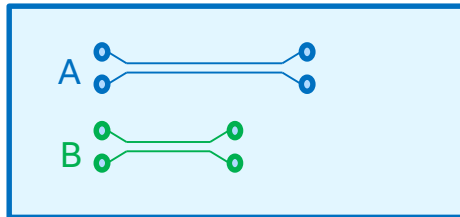
Reference: **Delta-L Methodology for Electrical Characterization, Rev. 330223-001**

<http://www.intel.com/content/www/us/en/processors/xeon/delta-l-methodology-for-electrical-characterization-guide.html>

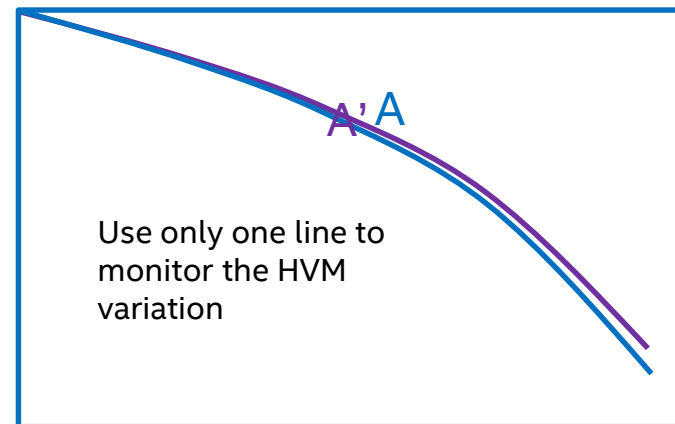
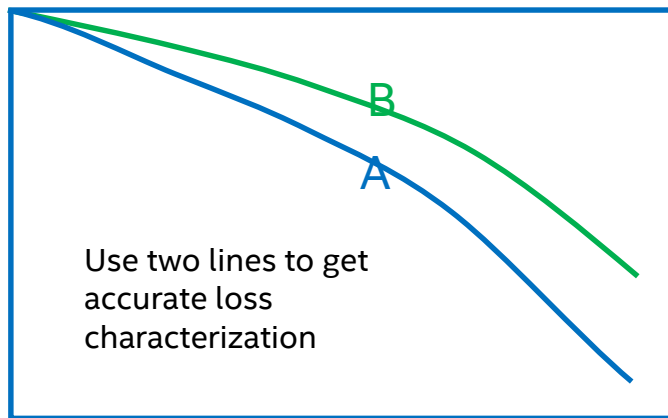
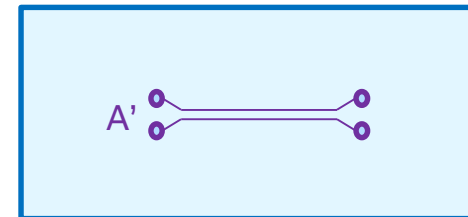
Delta-L+ (1L)

One-Line Method

Material Selection/
Board Sampling



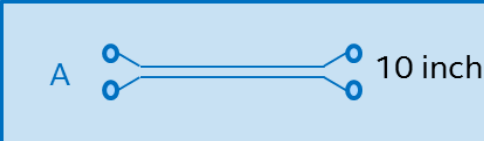
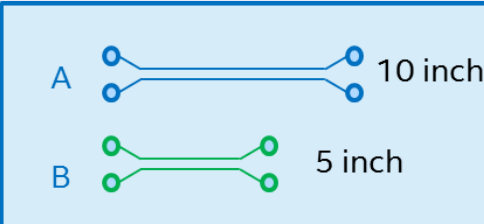
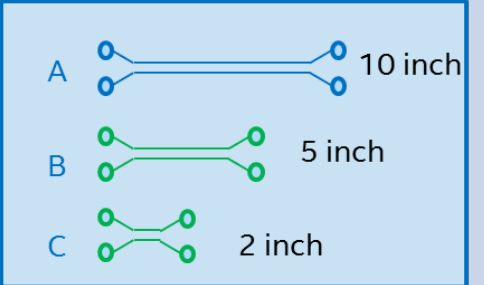
HVM Monitoring



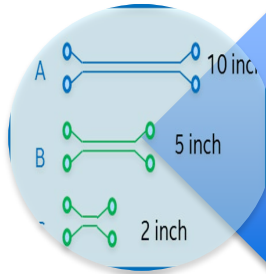
Keep track of performance of "A"

Criteria: < 10% (TBC) variation @ Nyquist frequency for at least x samples

Delta-L+ Usage Model

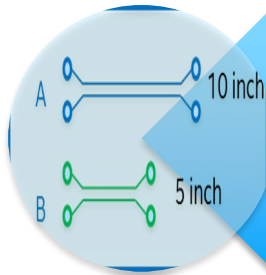
Category	Primary Usage	Note
<p>1L</p> 	<p>PCB house, HVM monitoring</p>	<p>Lowest cost solution, TDR/TDT or VNA is ok</p>
<p>2L</p> 	<p>PCB House (optional) OxM seeking low cost “de-embedding”</p>	<p>This is Delta-L 2.0, TDR/TDR or VNA is ok, VNA is preferred</p>
<p>3L</p> 	<p>Material vendor OxMs</p> <p>Any measurement capability verification</p>	<p>VNA preferred. Prefer rigorous de-embedding (AFR, SFD, TRL, etc.)</p>

Summary



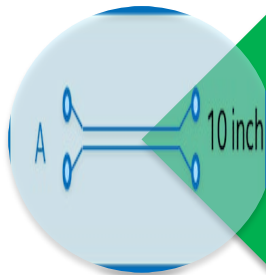
3L:

for best accuracy
Self-validation of results



2L:

cost effective approach to
remove test fixture impact



1L:

Focus on relative comparison
(for high volume manufacture)

