



Intel FPGA Triple Speed Ethernet IP Core Release Notes



Contents

1 Intel FPGA Triple Speed Ethernet IP Core Release Notes.....	3
1.1 Intel FPGA Triple Speed Ethernet IP Core v17.1.....	3
1.2 Triple Speed Ethernet IP Core v15.1.....	4
1.3 Triple Speed Ethernet IP Core v15.0.....	4
1.4 Triple Speed Ethernet IP Core v14.0 Arria 10 Edition.....	4
1.5 Triple Speed Ethernet IP Core v14.0.....	5
1.6 Triple Speed Ethernet IP Core v13.1 Arria 10 Edition.....	5
1.7 Triple Speed Ethernet IP Core v13.1	5



1 Intel FPGA Triple Speed Ethernet IP Core Release Notes

If a release note is not available for a specific IP core version, the IP core has no changes in that version. Information on the latest update releases is in the *Intel Quartus Prime Design Suite Update Release Notes*.

Related Links

[Intel Quartus Prime Design Suite Update Release Notes](#)

1.1 Intel FPGA Triple Speed Ethernet IP Core v17.1

Table 1. v17.1 November 2017

Description	Impact
Added support for the Intel® Stratix® 10, Intel Cyclone® 10 GX, and Intel Cyclone 10 LP device families.	These devices are only available in Intel Quartus® Prime Pro Edition software version 17.1 onwards.
In versions 17.0.2 and earlier of the Triple-Speed Ethernet IP core, the Triple-Speed Ethernet IP variant with LVDS I/O for PMA implementation in Intel Arria® 10 devices may experience performance risk. This issue is fixed in the Intel Quartus Prime software version 17.1.	To upgrade designs from previous versions of the Intel Quartus Prime software to version 17.1, you must regenerate the Triple-Speed Ethernet IP core and recompile the design in the Intel Quartus Prime software version 17.1. Refer to the KDB page for more information.
The number of ports supported for Triple-Speed Ethernet design with LVDS I/O targeting Intel Stratix 10, Intel Arria 10, and Intel Cyclone 10 GX is 8 per instance. You must not promote the reference clock to global clock manually. Assign the number of ports supported and its reference clock to the same I/O bank as inter-bank clock sharing is not allowed.	—
RGMII interface is not supported in Intel Stratix 10, Intel Arria 10, and Intel Cyclone 10 GX devices.	—

Related Links

- [Intel FPGA Triple Speed Ethernet IP Core User Guide](#)
- [Errata for Intel FPGA Triple Speed Ethernet IP core in the Knowledge Base](#)
- [KDB Link: Performance Risk Running Triple Speed Ethernet LVDS in Arria 10 Devices](#)

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1.2 Triple Speed Ethernet IP Core v15.1

Table 2. v15.1 November 2015

Description	Impact
Updated the ToD Clock module: <ul style="list-style-type: none">Added a new parameter—PERIOD_CLOCK_FREQUENCY.	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
Updated the ToD Synchronizer module: <ul style="list-style-type: none">Added a new parameter—SAMPLE SIZE.Changed the parameter value of SYNC_MODE to "Between 0 to 15".Changed the frequency range to 390.625 MHz.	

Related Links

- [Triple Speed Ethernet IP Core User Guide](#)
- [Errata for Triple Speed Ethernet IP core in the Knowledge Base](#)

1.3 Triple Speed Ethernet IP Core v15.0

Table 3. v15.0 May 2015

Description	Impact
You may observe hold time violation in designs targeting the Stratix V, Arria V, Cyclone V, and Arria 10 (10AS066ES) devices in this release.	Refer to the following errata for more information and the workaround: Hold Time Violation in Triple Speed Ethernet IP Core .

Related Links

- [Introduction to Altera IP Cores](#)
- [Triple Speed Ethernet MegaCore Function User Guide](#)
- [Errata for Triple Speed Ethernet IP core in the Knowledge Base](#)

1.4 Triple Speed Ethernet IP Core v14.0 Arria 10 Edition

Table 4. v14.0 Arria 10 Edition August 2014

Description	Impact
Verified in the Quartus II software v14.0 Arria 10 Edition. (Added support for Arria 10 devices).	If you upgrade your IP core to the Quartus II software v14.0 Arria 10 Edition, all of the changes require that you regenerate the IP core manually and reconnect it in your design.

Related Links

- [Introduction to Altera IP Cores](#)
- [Triple Speed Ethernet MegaCore Function User Guide](#)
- [Errata for Triple Speed Ethernet IP core in the Knowledge Base](#)



1.5 Triple Speed Ethernet IP Core v14.0

Table 5. v14.0 June 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to <i>IP Catalog and Parameter Editor</i> in <i>Introduction to Altera IP Cores</i> .	-
Added ECC support for M20K blocks.	Optional changes. If you do not upgrade your IP core, it does not have these new features:
Added 1588v2 support for LVDS variant.	

Related Links

- [Introduction to Altera IP Cores](#)
- [Triple Speed Ethernet MegaCore Function User Guide](#)
- [Errata for Triple Speed Ethernet IP core in the Knowledge Base](#)

1.6 Triple Speed Ethernet IP Core v13.1 Arria 10 Edition

Table 6. v13.1 Arria 10 Edition December 2014

Description	impact
Added support for Arria 10 devices.	-

Related Links

- [Introduction to Altera IP Cores](#)
- [Triple Speed Ethernet MegaCore Function User Guide](#)
- [Errata for Triple Speed Ethernet IP core in the Knowledge Base](#)

1.7 Triple Speed Ethernet IP Core v13.1

Table 7. v13.1 November 2013

Description	Impact
Removed support for the following devices: <ul style="list-style-type: none"> • Arria GX • Cyclone II • HardCopy II, HardCopy III, and HardCopy IV • Stratix II and Stratix II GX 	-
Added 1588v2 support for Arria V, Arria V SoC, Cyclone V, Cyclone V SoC and Stratix V devices.	-
Added 1588v2 support for MAC-only variants	-
Added ATX and CMU Tx PLL options for variations that include the PCS block targeting Arria V GZ and Stratix V devices.	-
Added SyncE support by separating Tx PLL and Rx PLL reference clock.	-
The period in nanosecond for csr registers: <code>tx_period</code> , <code>rx_period</code> , <code>Period</code> , and <code>AdjustPeriod</code> , was changed from bit 16 to 19 to bit 16 to 24.	-



Related Links

- [Introduction to Altera IP Cores](#)
- [Triple Speed Ethernet MegaCore Function User Guide](#)
- [Errata for Triple Speed Ethernet IP core in the Knowledge Base](#)