MAX V CPLD Features

View device ordering codes on **page 40**.

		MAX V CPLDs (1.8 V)						
		5M40Z	5M80Z	5M160Z	5M240Z	5M570Z	5M1270Z	5M2210Z
Density and Speed	LEs	40	80	160	240	570	1270	2210
	Equivalent macrocells[1]	32	64	128	192	440	980	1700
	Pin-to-pin delay (ns)	7.5	7.5	7.5	7.5	9.0	6.2	7.0
	User flash memory (Kb)	8						
	Total on-chip memory (bits)[2]	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Architectural Features	Internal oscillator	✓						
	Digital PLL[3]	✓						
	Fast power-on reset	✓						
	Boundary-scan JTAG	✓						
	JTAG ISP	✓						
	Fast input registers	✓						
	Programmable register power-up	✓						
	JTAG translator	✓						
	Real-time ISP	✓						
I/O Features	MultiVolt I/Os (V)	1.2, 1.5, 1.8, 2.5, 3.3					1.2, 1.5, 1.8, 2.5, 3.3, 5.0[4]	
	I/O power banks	2	2	2	2	2	4	4
	Maximum output enables	54	54	79	114	159	271	271
	LVTTL/LVCMOS	✓						
	LVDS outputs	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	32 bit, 66 MHz PCI compliant	–	–	–	–	–	✓[4]	✓[4]
	Schmitt triggers	✓						
	Programmable slew rate	✓						
	Programmable pull-up resistors	✓						
	Programmable GND pins	✓						
	Open-drain outputs	✓						
	Bus hold	✓						

Notes:

1. Typical equivalent macrocells.
2. Unused LEs can be converted to memory. The total number of available LE RAM bits depends on the memory mode, depth, and width configurations of the instantiated memory.
3. Optional IP core. Contact your Altera sales representative for availability.
4. An external resistor must be used for 5.0 V tolerance.