**Revision 1.1.0**
**ADV Issue Date: 01/10/2020**
**Rev 1.1.0 Date: 03/13/2020**

# CUSTOMER ADVISORY

# ADV2003

## Intel® Arria® 10 Device EDCRC and Partial Reconfiguration Update

**This is not a new ADV issuance. This is an update to ADV2003; please see the revision history table for information specific to this update.**

## Description:

Intel® is notifying customers of potential problems in selected Intel Arria® 10 devices when Error Detection Cyclic Redundancy Check (EDCRC) is On or Partial Reconfiguration (PR) is used.

Failure signature: Unexpected output from Flipflop/DSP/M20k/LUTRAM when EDCRC or PR is used. The problems will not occur if EDCRC or PR is turned-off.

**Table 1**

| Cause 1: | Recommended Action: |
|---|---|
| Functional failure if clock components (Flipflop/DSP/M20k/LUTRAM) are placed in LAB row Y59, with EDCRC On or PR enabled. | Implement software fix in Intel Quartus® Prime software.<br>For more details on the software fix refer to the following Knowledge Database via this link: https://www.intel.com/content/altera-www/global/en_us/index/support/support-resources/knowledge-base/component/2019/is-there-a-problem-with-intel--fpga-when-flipflop-dsp-m20k-lutra.html |

<table>
<tr><th>Cause 2:</th><th>Recommended Action:</th></tr>
<tr><td>Functional failure if clock components (Flipflop/DSP/M20k/LUTRAM) are placed in a random LAB row, with EDCRC On or PR enabled. This is caused by unoptimized internal voltage VCCHG value in test.</td><td>The optimized VCCHG value will be implemented according to the datecodes below:<br><br><table><tr><td>Device Density/OPN</td><td>Fix implementation starting datecode</td></tr><tr><td>GX270/GX320/SX270/SX320</td><td>2025(Year 2020; WW25)</td></tr><tr><td>GX160/GX220/SX160/SX220</td><td>2025(Year 2020; WW25)</td></tr></table>Note: Part numbers (OPNs) with corresponding fix implementation datecode is in the “Products Affected” link below.<br><br>For parts before the above datecodes, there is no action required. Failure rate has been assessed to be very low (~20dppm).</td></tr>
</table>

For questions or support, please contact your local Field Applications Engineer (FAE) or submit a service request in the My Intel support page.

## Products Affected:

All part numbers for the device densities listed below per product family.

| Product Family | Device Density |
|---|---|
| Arria 10 GX | GX160/GX220/GX270/GX320 |
| Arria 10 SX | SX160/SX220/SX270/SX320 |

**The list of affected part numbers (OPNs) can be downloaded in Excel form:**
https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/pcn/adv2003-opn-list.xlsx

## Reason for Change:

Due to potential problems discovered in selected Intel Arria 10 devices using the EDCRC/PR feature, the above update was needed to help customers mitigate it. There is no change to the Intel Arria 10 device silicon and materials.

## Change Implementation:

| Milestone | Availability |
|---|---|
| Availability of error message in Intel Quartus Prime software version 18.1.1 and above, if EDCRC and/or PR usage is detected without implementing software fix.<br>Refer to the following KDB link for more details on the error message. https://www.intel.com/content/altera-www/global/en_us/index/support/support-resources/knowledge-base/component/2019/is-there-a-problem-with-intel--fpga-when-flipflop-dsp-m20k-lutra.html | Now |
| Availability of optimized internal voltage VCCHG fix in affected Intel Arria 10 devices | Refer Table 1 |

## Contact:

For more information, please contact your local Field Applications Engineer (FAE) or submit a Service Request at the My Intel support page.

## Customer Notifications Subscription:

Customers that subscribe to Intel PSG's customer notification mailing list can receive the Customer Advisory automatically via email.

If you would like to receive customer notifications by email, please subscribe to our customer notification mailing list at:
https://www.intel.com/content/www/us/en/programmable/my-intel/mal-emailsub/technical-updates.html

## Revision History:

| Date | Rev | Description |
|---|---|---|
| 01/10/2020 | 1.0.0 | Initial Release |
| 03/13/2020 | 1.1.0 | Revised implementation datecode from 2013 to 2025 [Table 1: Fix implementation starting datecode for Device Density/OPN GX270/GX320/SX270/SX320 is 2025(Year 2020; WW25)] |