Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896 *(3)*	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36	DDR3/DDR2 Hard Memory PHY *(4)*
		DNU					E29				
		DNU					F29				
		RREF_TL					F30				
GXB_L1		GXB_TX_L8n					G27*				
GXB_L1		GXB_TX_L8p					G28*				
GXB_L1		GXB_RX_L8p,GXB_REFCLK_L8p					H30*				
GXB_L1		GXB_RX_L8n,GXB_REFCLK_L8n					H29*				
GXB_L1		GXB_TX_L7n					J27				
GXB_L1		GXB_TX_L7p					J28				
GXB_L1		GXB_RX_L7p,GXB_REFCLK_L7p					K30				
GXB_L1		GXB_RX_L7n,GXB_REFCLK_L7n					K29				
GXB_L1		GXB_TX_L6n					L27*				
GXB_L1		GXB_TX_L6p					L28*				
GXB_L1		GXB_RX_L6p,GXB_REFCLK_L6p					M30*				
GXB_L1		GXB_RX_L6n,GXB_REFCLK_L6n					M29*				
GXB_L1		REFCLK2Ln					R23				
GXB_L1		REFCLK2Lp					R22				
GXB_L0		REFCLK1Ln					U23				
GXB_L0		REFCLK1Lp					U22				
GXB_L0		GXB_TX_L5n					N27*				
GXB_L0		GXB_TX_L5p					N28*				
GXB_L0		GXB_RX_L5p,GXB_REFCLK_L5p					P30*				
GXB_L0		GXB_RX_L5n,GXB_REFCLK_L5n					P29*				
GXB_L0		GXB_TX_L4n					R27				
GXB_L0		GXB_TX_L4p					R28				
GXB_L0		GXB_RX_L4p,GXB_REFCLK_L4p					T30				
GXB_L0		GXB_RX_L4n,GXB_REFCLK_L4n					T29				
GXB_L0		GXB_TX_L3n					U27*				
GXB_L0		GXB_TX_L3p					U28*				
GXB_L0		GXB_RX_L3p,GXB_REFCLK_L3p					V30*				
GXB_L0		GXB_RX_L3n,GXB_REFCLK_L3n					V29*				
GXB_L0		GXB_TX_L2n					W27				
GXB_L0		GXB_TX_L2p					W28				
GXB_L0		GXB_RX_L2p,GXB_REFCLK_L2p					Y30				
GXB_L0		GXB_RX_L2n,GXB_REFCLK_L2n					Y29				
GXB_L0		GXB_TX_L1n					AA27				
GXB_L0		GXB_TX_L1p					AA28				
GXB_L0		GXB_RX_L1p,GXB_REFCLK_L1p					AB30				
GXB_L0		GXB_RX_L1n,GXB_REFCLK_L1n					AB29				
GXB_L0		GXB_TX_L0n					AC27*				
GXB_L0		GXB_TX_L0p					AC28*				
GXB_L0		GXB_RX_L0p,GXB_REFCLK_L0p					AD30*				
GXB_L0		GXB_RX_L0n,GXB_REFCLK_L0n					AD29*				
GXB_L0		REFCLK0Ln					W23				
GXB_L0		REFCLK0Lp					W22				
		DNU					AB26				
3A		TDO		TDO			AF30				
3A		TMS		TMS			AG30				
3A		TCK		TCK			AG29				
3A		TDI		TDI			AF29				
3A		DCLK		DCLK			AJ29				
3A		nCSO		DATA4			AA25				
3A		AS_DATA3		DATA3			AH30				
3A		AS_DATA2		DATA2			AJ30				
3A		AS_DATA1		DATA1			AK29				
3A		AS_DATA0,ASDO		DATA0			AK28				
3A	VREFB3AN0	IO	RZQ_0		DIFFIO_TX_B1n	DIFFOUT_B1n	AF28				
3A	VREFB3AN0	IO			DIFFIO_TX_B1p	DIFFOUT_B1p	AG28	DQ1B			
3A	VREFB3AN0	IO	CLK0n		DIFFIO_RX_B2n	DIFFOUT_B2n	AF27	DQ1B			
3A	VREFB3AN0	IO	CLK0p		DIFFIO_RX_B2p	DIFFOUT_B2p	AG27	DQ1B			
3A	VREFB3AN0	IO			DIFFIO_TX_B3n	DIFFOUT_B3n	AE27				
3A	VREFB3AN0	IO			DIFFIO_TX_B3p	DIFFOUT_B3p	AE26	DQ1B			
3A	VREFB3AN0	IO	CLK1n		DIFFIO_RX_B4n	DIFFOUT_B4n	AH28	DQSn1B/QK1B			
3A	VREFB3AN0	IO	CLK1p		DIFFIO_RX_B4p	DIFFOUT_B4p	AJ28	DQS1B/CQ1B/CQn1B/QKn1B			
3A	VREFB3AN0	IO	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO_TX_B5n	DIFFOUT_B5n	AJ27				
3A	VREFB3AN0	IO	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB0		DIFFIO_TX_B5p	DIFFOUT_B5p	AK27	DQ1B			
3A	VREFB3AN0	IO	FPLL_BL_CLKOUT3,FPLL_BL_FBn		DIFFIO_RX_B6n	DIFFOUT_B6n	AB25	DQ1B			
3A	VREFB3AN0	IO	FPLL_BL_CLKOUT2,FPLL_BL_FBp,FPLL_BL_FB1		DIFFIO_RX_B6p	DIFFOUT_B6p	AC25	DQ1B			
3A	VREFB3AN0	IO	VREFB3AN0				AD25				
3A	VREFB3AN0	IO					AE25	DQ1B			
3A	VREFB3AN0	IO	CLK2n		DIFFIO_RX_B7n	DIFFOUT_B7n	AG26	DQ1B			
3A	VREFB3AN0	IO	CLK2p		DIFFIO_RX_B7p	DIFFOUT_B7p	AH26	DQ1B			
3A	VREFB3AN0	IO			DIFFIO_TX_B8n	DIFFOUT_B8n	AK26				
3A	VREFB3AN0	IO			DIFFIO_TX_B8p	DIFFOUT_B8p	AK25	DQ2B			
3A	VREFB3AN0	IO	CLK3n		DIFFIO_RX_B9n	DIFFOUT_B9n	AF25	DQ2B			
3A	VREFB3AN0	IO	CLK3p		DIFFIO_RX_B9p	DIFFOUT_B9p	AG25	DQ2B			
3A	VREFB3AN0	IO			DIFFIO_TX_B10n	DIFFOUT_B10n	AB23				
3A	VREFB3AN0	IO			DIFFIO_TX_B10p	DIFFOUT_B10p	AB24	DQ2B			
3A	VREFB3AN0	IO			DIFFIO_RX_B11n	DIFFOUT_B11n	AH25	DQSn2B/QK2B			
3A	VREFB3AN0	IO			DIFFIO_RX_B11p	DIFFOUT_B11p	AJ25	DQS2B/CQ2B/CQn2B/QKn2B			
3A	VREFB3AN0	IO			DIFFIO_TX_B12n	DIFFOUT_B12n	AC24				
3A	VREFB3AN0	IO			DIFFIO_TX_B12p	DIFFOUT_B12p	AD24	DQ2B			
3A	VREFB3AN0	IO			DIFFIO_RX_B13n	DIFFOUT_B13n	AF24	DQ2B			
3A	VREFB3AN0	IO			DIFFIO_RX_B13p	DIFFOUT_B13p	AG24	DQ2B			
3A	VREFB3AN0	IO			DIFFIO_TX_B14n	DIFFOUT_B14n	AD23				
3A	VREFB3AN0	IO			DIFFIO_TX_B14p	DIFFOUT_B14p	AE23	DQ2B			
3A	VREFB3AN0	IO			DIFFIO_RX_B15n	DIFFOUT_B15n	AJ24	DQ2B			
3A	VREFB3AN0	IO			DIFFIO_RX_B15p	DIFFOUT_B15p	AK24	DQ2B			
3D	VREFB3DN0	IO			DIFFIO_TX_B54n	DIFFOUT_B54n	AC22				
3D	VREFB3DN0	IO			DIFFIO_TX_B54p	DIFFOUT_B54p	AD22	DQ3B	DQ1B		
3D	VREFB3DN0	IO			DIFFIO_RX_B55n	DIFFOUT_B55n	AA22	DQ3B	DQ1B		
3D	VREFB3DN0	IO			DIFFIO_RX_B55p	DIFFOUT_B55p	AB22	DQ3B	DQ1B		
3D	VREFB3DN0	IO			DIFFIO_TX_B56n	DIFFOUT_B56n	AB21				
3D	VREFB3DN0	IO			DIFFIO_TX_B56p	DIFFOUT_B56p	AC21	DQ3B	DQ1B		

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896 *(3)*	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36	DDR3/DDR2 Hard Memory PHY *(4)*
3D	VREFB3DN0	IO			DIFFIO_RX_B57n	DIFFOUT_B57n	AG23	DQSn3B/QK3B	DQ1B		
3D	VREFB3DN0	IO			DIFFIO_RX_B57p	DIFFOUT_B57p	AH23	DQS3B/CQ3B/CQn3B/QKn3B	DQ1B		
3D	VREFB3DN0	IO			DIFFIO_TX_B58n	DIFFOUT_B58n	AD21				
3D	VREFB3DN0	IO			DIFFIO_TX_B58p	DIFFOUT_B58p	AE22	DQ3B	DQ1B		
3D	VREFB3DN0	IO			DIFFIO_RX_B59n	DIFFOUT_B59n	AF22	DQ3B	DQ1B		
3D	VREFB3DN0	IO			DIFFIO_RX_B59p	DIFFOUT_B59p	AG22	DQ3B	DQ1B		
3D	VREFB3DN0	IO	VREFB3DN0				AA21				
3D	VREFB3DN0	IO					Y20	DQ3B	DQ1B		
3D	VREFB3DN0	IO	CLK4n		DIFFIO_RX_B60n	DIFFOUT_B60n	AH22	DQ3B	DQ1B		
3D	VREFB3DN0	IO	CLK4p		DIFFIO_RX_B60p	DIFFOUT_B60p	AJ22	DQ3B	DQ1B		
3D	VREFB3DN0	IO			DIFFIO_TX_B61n	DIFFOUT_B61n	AD20				
3D	VREFB3DN0	IO			DIFFIO_TX_B61p	DIFFOUT_B61p	AE20	DQ4B	DQ1B		
3D	VREFB3DN0	IO	CLK5n		DIFFIO_RX_B62n	DIFFOUT_B62n	AF21	DQ4B	DQ1B		
3D	VREFB3DN0	IO	CLK5p		DIFFIO_RX_B62p	DIFFOUT_B62p	AG21	DQ4B	DQ1B		
3D	VREFB3DN0	IO	FPLL_BC_CLKOUT1,FPLL_BC_CLKOUTn		DIFFIO_TX_B63n	DIFFOUT_B63n	AA19				
3D	VREFB3DN0	IO	FPLL_BC_CLKOUT0,FPLL_BC_CLKOUTp,FPLL_BC_FB0		DIFFIO_TX_B63p	DIFFOUT_B63p	AB19	DQ4B	DQ1B		
3D	VREFB3DN0	IO	FPLL_BC_CLKOUT3,FPLL_BC_FBn		DIFFIO_RX_B64n	DIFFOUT_B64n	AG20	DQSn4B/QK4B	DQSn1B/QK1B		
3D	VREFB3DN0	IO	FPLL_BC_CLKOUT2,FPLL_BC_FBp,FPLL_BC_FB1		DIFFIO_RX_B64p	DIFFOUT_B64p	AH20	DQS4B/CQ4B/CQn4B/QKn4B	DQS1B/CQ1B/CQn1B/QKn1B		
3D	VREFB3DN0	IO			DIFFIO_TX_B65n	DIFFOUT_B65n	AA20				
3D	VREFB3DN0	IO			DIFFIO_TX_B65p	DIFFOUT_B65p	AB20	DQ4B	DQ1B		
3D	VREFB3DN0	IO	CLK6n		DIFFIO_RX_B66n	DIFFOUT_B66n	AJ21	DQ4B	DQ1B		
3D	VREFB3DN0	IO	CLK6p		DIFFIO_RX_B66p	DIFFOUT_B66p	AK22	DQ4B	DQ1B		
3D	VREFB3DN0	IO			DIFFIO_TX_B67n	DIFFOUT_B67n	AC19				
3D	VREFB3DN0	IO			DIFFIO_TX_B67p	DIFFOUT_B67p	AD19	DQ4B	DQ1B		
3D	VREFB3DN0	IO	CLK7n		DIFFIO_RX_B68n	DIFFOUT_B68n	AK20	DQ4B	DQ1B		
3D	VREFB3DN0	IO	CLK7p		DIFFIO_RX_B68p	DIFFOUT_B68p	AK21	DQ4B	DQ1B		
		VCCD_FPLL					W15				
		VCCA_FPLL					W16				
		DNU					Y16				
4D	VREFB4DN0	IO			DIFFIO_TX_B69n	DIFFOUT_B69n	AJ19				CS#_4D_1
4D	VREFB4DN0	IO			DIFFIO_TX_B69p	DIFFOUT_B69p	AK19	DQ5B	DQ2B		CS#_4D_0
4D	VREFB4DN0	IO			DIFFIO_RX_B70n	DIFFOUT_B70n	AF19	DQ5B	DQ2B		
4D	VREFB4DN0	IO			DIFFIO_RX_B70p	DIFFOUT_B70p	AG19	DQ5B	DQ2B		A_4D_15
4D	VREFB4DN0	IO			DIFFIO_TX_B71n	DIFFOUT_B71n	AC18				ODT_4D_1
4D	VREFB4DN0	IO			DIFFIO_TX_B71p	DIFFOUT_B71p	AD18	DQ5B	DQ2B		ODT_4D_0
4D	VREFB4DN0	IO			DIFFIO_RX_B72n	DIFFOUT_B72n	AH19	DQSn5B/QK5B	DQ2B		WE#_4D
4D	VREFB4DN0	IO			DIFFIO_RX_B72p	DIFFOUT_B72p	AH18	DQS5B/CQ5B/CQn5B/QKn5B	DQ2B		CAS#_4D
4D	VREFB4DN0	IO			DIFFIO_TX_B73n	DIFFOUT_B73n	AA18				RAS#_4D
4D	VREFB4DN0	IO			DIFFIO_TX_B73p	DIFFOUT_B73p	AB18	DQ5B	DQ2B		BA_4D_2
4D	VREFB4DN0	IO			DIFFIO_RX_B74n	DIFFOUT_B74n	AE18	DQ5B	DQ2B		BA_4D_1
4D	VREFB4DN0	IO			DIFFIO_RX_B74p	DIFFOUT_B74p	AF18	DQ5B	DQ2B		BA_4D_0
4D	VREFB4DN0	IO	VREFB4DN0				AD17				
4D	VREFB4DN0	IO					AE17	DQ5B	DQ2B		A_4D_14
4D	VREFB4DN0	IO			DIFFIO_RX_B75n	DIFFOUT_B75n	AA17	DQ5B	DQ2B		A_4D_13
4D	VREFB4DN0	IO			DIFFIO_RX_B75p	DIFFOUT_B75p	AB17	DQ5B	DQ2B		A_4D_12
4D	VREFB4DN0	IO			DIFFIO_TX_B76n	DIFFOUT_B76n	AA16				A_4D_11
4D	VREFB4DN0	IO			DIFFIO_TX_B76p	DIFFOUT_B76p	AB16	DQ6B	DQ2B		A_4D_10
4D	VREFB4DN0	IO			DIFFIO_RX_B77n	DIFFOUT_B77n	AG17	DQ6B	DQ2B		A_4D_9
4D	VREFB4DN0	IO			DIFFIO_RX_B77p	DIFFOUT_B77p	AH17	DQ6B	DQ2B		A_4D_8
4D	VREFB4DN0	IO			DIFFIO_TX_B78n	DIFFOUT_B78n	AC16				A_4D_7
4D	VREFB4DN0	IO			DIFFIO_TX_B78p	DIFFOUT_B78p	AD16	DQ6B	DQ2B		A_4D_6
4D	VREFB4DN0	IO			DIFFIO_RX_B79n	DIFFOUT_B79n	AJ18	DQSn6B/QK6B	DQSn2B/QK2B		A_4D_5
4D	VREFB4DN0	IO			DIFFIO_RX_B79p	DIFFOUT_B79p	AK17	DQS6B/CQ6B/CQn6B/QKn6B	DQS2B/CQ2B/CQn2B/QKn2B		A_4D_4
4D	VREFB4DN0	IO			DIFFIO_TX_B80n	DIFFOUT_B80n	AF16				A_4D_3
4D	VREFB4DN0	IO			DIFFIO_TX_B80p	DIFFOUT_B80p	AG16	DQ6B	DQ2B		A_4D_2
4D	VREFB4DN0	IO			DIFFIO_RX_B81n	DIFFOUT_B81n	AA15	DQ6B	DQ2B		A_4D_1
4D	VREFB4DN0	IO			DIFFIO_RX_B81p	DIFFOUT_B81p	AB15	DQ6B	DQ2B		A_4D_0
4D	VREFB4DN0	IO			DIFFIO_TX_B82n	DIFFOUT_B82n	AC15				CKE_4D_1
4D	VREFB4DN0	IO			DIFFIO_TX_B82p	DIFFOUT_B82p	AD15	DQ6B	DQ2B		CKE_4D_0
4D	VREFB4DN0	IO			DIFFIO_RX_B83n	DIFFOUT_B83n	AJ16	DQ6B	DQ2B		CK#_4D
4D	VREFB4DN0	IO			DIFFIO_RX_B83p	DIFFOUT_B83p	AK16	DQ6B	DQ2B		CK_4D
4C	VREFB4CN0	IO			DIFFIO_TX_B84n	DIFFOUT_B84n	AA14				RESET#_4D
4C	VREFB4CN0	IO			DIFFIO_TX_B84p	DIFFOUT_B84p	AB14	DQ7B	DQ3B	DQ1B	DQ1_4C_8
4C	VREFB4CN0	IO			DIFFIO_RX_B85n	DIFFOUT_B85n	AG15	DQ7B	DQ3B	DQ1B	DQ1_4C_7
4C	VREFB4CN0	IO			DIFFIO_RX_B85p	DIFFOUT_B85p	AH15	DQ7B	DQ3B	DQ1B	DQ1_4C_6
4C	VREFB4CN0	IO			DIFFIO_TX_B86n	DIFFOUT_B86n	AE15				
4C	VREFB4CN0	IO			DIFFIO_TX_B86p	DIFFOUT_B86p	AF15	DQ7B	DQ3B	DQ1B	DM1_4C
4C	VREFB4CN0	IO			DIFFIO_RX_B87n	DIFFOUT_B87n	AJ15	DQSn7B/QK7B	DQ3B	DQ1B	DQS#1_4C
4C	VREFB4CN0	IO			DIFFIO_RX_B87p	DIFFOUT_B87p	AK14	DQS7B/CQ7B/CQn7B/QKn7B	DQ3B	DQ1B	DQS1_4C
4C	VREFB4CN0	IO			DIFFIO_TX_B88n	DIFFOUT_B88n	AG14				
4C	VREFB4CN0	IO			DIFFIO_TX_B88p	DIFFOUT_B88p	AH14	DQ7B	DQ3B	DQ1B	DQ1_4C_5
4C	VREFB4CN0	IO			DIFFIO_RX_B89n	DIFFOUT_B89n	AD13	DQ7B	DQ3B	DQ1B	DQ1_4C_4
4C	VREFB4CN0	IO			DIFFIO_RX_B89p	DIFFOUT_B89p	AE13	DQ7B	DQ3B	DQ1B	DQ1_4C_3
4C	VREFB4CN0	IO	VREFB4CN0				AD14				
4C	VREFB4CN0	IO					AE14	DQ7B	DQ3B	DQ1B	DQ1_4C_2
4C	VREFB4CN0	IO			DIFFIO_RX_B90n	DIFFOUT_B90n	AH13	DQ7B	DQ3B	DQ1B	DQ1_4C_1
4C	VREFB4CN0	IO			DIFFIO_RX_B90p	DIFFOUT_B90p	AJ13	DQ7B	DQ3B	DQ1B	DQ1_4C_0
4C	VREFB4CN0	IO			DIFFIO_TX_B91n	DIFFOUT_B91n	AC13				
4C	VREFB4CN0	IO			DIFFIO_TX_B91p	DIFFOUT_B91p	AD12	DQ8B	DQ3B	DQ1B	DQ2_4C_8
4C	VREFB4CN0	IO			DIFFIO_RX_B92n	DIFFOUT_B92n	AF12	DQ8B	DQ3B	DQ1B	DQ2_4C_7
4C	VREFB4CN0	IO			DIFFIO_RX_B92p	DIFFOUT_B92p	AF13	DQ8B	DQ3B	DQ1B	DQ2_4C_6
4C	VREFB4CN0	IO			DIFFIO_TX_B93n	DIFFOUT_B93n	AA13				
4C	VREFB4CN0	IO			DIFFIO_TX_B93p	DIFFOUT_B93p	AB13	DQ8B	DQ3B	DQ1B	DM2_4C
4C	VREFB4CN0	IO			DIFFIO_RX_B94n	DIFFOUT_B94n	AG12	DQSn8B/QK8B	DQSn3B/QK3B	DQ1B	DQS#2_4C
4C	VREFB4CN0	IO			DIFFIO_RX_B94p	DIFFOUT_B94p	AH12	DQS8B/CQ8B/CQn8B/QKn8B	DQS3B/CQ3B/CQn3B/QKn3B	DQ1B	DQS2_4C
4C	VREFB4CN0	IO			DIFFIO_TX_B95n	DIFFOUT_B95n	AJ12				
4C	VREFB4CN0	IO			DIFFIO_TX_B95p	DIFFOUT_B95p	AK12	DQ8B	DQ3B	DQ1B	DQ2_4C_5
4C	VREFB4CN0	IO			DIFFIO_RX_B96n	DIFFOUT_B96n	AB12	DQ8B	DQ3B	DQ1B	DQ2_4C_4
4C	VREFB4CN0	IO			DIFFIO_RX_B96p	DIFFOUT_B96p	AC12	DQ8B	DQ3B	DQ1B	DQ2_4C_3
4C	VREFB4CN0	IO			DIFFIO_TX_B97n	DIFFOUT_B97n	Y12				
4C	VREFB4CN0	IO			DIFFIO_TX_B97p	DIFFOUT_B97p	Y13	DQ8B	DQ3B	DQ1B	DQ2_4C_2
4C	VREFB4CN0	IO			DIFFIO_RX_B98n	DIFFOUT_B98n	AG11	DQ8B	DQ3B	DQ1B	DQ2_4C_1
4C	VREFB4CN0	IO			DIFFIO_RX_B98p	DIFFOUT_B98p	AH11	DQ8B	DQ3B	DQ1B	DQ2_4C_0
4B	VREFB4BN0	IO			DIFFIO_TX_B99n	DIFFOUT_B99n	AD11				

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896 *(3)*	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36	DDR3/DDR2 Hard Memory PHY *(4)*
4B	VREFB4BN0	IO			DIFFIO_TX_B99p	DIFFOUT_B99p	AE11	DQ9B	DQ4B	DQ1B	DQ3_4B_8
4B	VREFB4BN0	IO			DIFFIO_RX_B100n	DIFFOUT_B100n	AA12	DQ9B	DQ4B	DQ1B	DQ3_4B_7
4B	VREFB4BN0	IO			DIFFIO_RX_B100p	DIFFOUT_B100p	AB11	DQ9B	DQ4B	DQ1B	DQ3_4B_6
4B	VREFB4BN0	IO			DIFFIO_TX_B101n	DIFFOUT_B101n	AA11				
4B	VREFB4BN0	IO			DIFFIO_TX_B101p	DIFFOUT_B101p	AA10	DQ9B	DQ4B	DQ1B	DM3_4B
4B	VREFB4BN0	IO			DIFFIO_RX_B102n	DIFFOUT_B102n	AK11	DQSn9B/QK9B	DQ4B	DQSn1B/QK1B	DQS#3_4B
4B	VREFB4BN0	IO			DIFFIO_RX_B102p	DIFFOUT_B102p	AK10	DQS9B/CQ9B/CQn9B/QKn9B	DQ4B	DQS1B/CQ1B/CQn1B/QKn1B	DQS3_4B
4B	VREFB4BN0	IO			DIFFIO_TX_B103n	DIFFOUT_B103n	AF10				
4B	VREFB4BN0	IO			DIFFIO_TX_B103p	DIFFOUT_B103p	AG10	DQ9B	DQ4B	DQ1B	DQ3_4B_5
4B	VREFB4BN0	IO			DIFFIO_RX_B104n	DIFFOUT_B104n	AB10	DQ9B	DQ4B	DQ1B	DQ3_4B_4
4B	VREFB4BN0	IO			DIFFIO_RX_B104p	DIFFOUT_B104p	AB9	DQ9B	DQ4B	DQ1B	DQ3_4B_3
4B	VREFB4BN0	IO			DIFFIO_TX_B105n	DIFFOUT_B105n	AC10				
4B	VREFB4BN0	IO			DIFFIO_TX_B105p	DIFFOUT_B105p	AD10	DQ9B	DQ4B	DQ1B	DQ3_4B_2
4B	VREFB4BN0	IO			DIFFIO_RX_B106n	DIFFOUT_B106n	AH9	DQ9B	DQ4B	DQ1B	DQ3_4B_1
4B	VREFB4BN0	IO			DIFFIO_RX_B106p	DIFFOUT_B106p	AJ10	DQ9B	DQ4B	DQ1B	DQ3_4B_0
4B	VREFB4BN0	IO			DIFFIO_TX_B107n	DIFFOUT_B107n	AE9				
4B	VREFB4BN0	IO			DIFFIO_TX_B107p	DIFFOUT_B107p	AF9	DQ10B	DQ4B	DQ1B	DQ4_4B_8
4B	VREFB4BN0	IO			DIFFIO_RX_B108n	DIFFOUT_B108n	AJ9	DQ10B	DQ4B	DQ1B	DQ4_4B_7
4B	VREFB4BN0	IO			DIFFIO_RX_B108p	DIFFOUT_B108p	AK8	DQ10B	DQ4B	DQ1B	DQ4_4B_6
4B	VREFB4BN0	IO			DIFFIO_TX_B109n	DIFFOUT_B109n	AC9				
4B	VREFB4BN0	IO			DIFFIO_TX_B109p	DIFFOUT_B109p	AD9	DQ10B	DQ4B	DQ1B	DM4_4B
4B	VREFB4BN0	IO			DIFFIO_RX_B110n	DIFFOUT_B110n	AA9	DQSn10B/QK10B	DQSn4B/QK4B	DQ1B	DQS#4_4B
4B	VREFB4BN0	IO			DIFFIO_RX_B110p	DIFFOUT_B110p	AB8	DQS10B/CQ10B/CQn10B/QKn10B	DQS4B/CQ4B/CQn4B/QKn4B	DQ1B	DQS4_4B
4B	VREFB4BN0	IO			DIFFIO_TX_B111n	DIFFOUT_B111n	AG8				
4B	VREFB4BN0	IO			DIFFIO_TX_B111p	DIFFOUT_B111p	AH8	DQ10B	DQ4B	DQ1B	DQ4_4B_5
4B	VREFB4BN0	IO			DIFFIO_RX_B112n	DIFFOUT_B112n	AJ7	DQ10B	DQ4B	DQ1B	DQ4_4B_4
4B	VREFB4BN0	IO			DIFFIO_RX_B112p	DIFFOUT_B112p	AK7	DQ10B	DQ4B	DQ1B	DQ4_4B_3
4B	VREFB4BN0	IO	VREFB4BN0				AD8				
4B	VREFB4BN0	IO					AE8	DQ10B	DQ4B	DQ1B	DQ4_4B_2
4B	VREFB4BN0	IO			DIFFIO_RX_B113n	DIFFOUT_B113n	AG7	DQ10B	DQ4B	DQ1B	DQ4_4B_1
4B	VREFB4BN0	IO			DIFFIO_RX_B113p	DIFFOUT_B113p	AH7	DQ10B	DQ4B	DQ1B	DQ4_4B_0
4A	VREFB4AN0	IO		DATA10	DIFFIO_TX_B114n	DIFFOUT_B114n	AF7				
4A	VREFB4AN0	IO		DATA11	DIFFIO_TX_B114p	DIFFOUT_B114p	AG6	DQ11B	DQ5B		
4A	VREFB4AN0	IO		DATA5	DIFFIO_RX_B115n	DIFFOUT_B115n	AJ6	DQ11B	DQ5B		
4A	VREFB4AN0	IO		DATA6	DIFFIO_RX_B115p	DIFFOUT_B115p	AK6	DQ11B	DQ5B		
4A	VREFB4AN0	IO		DATA12	DIFFIO_TX_B116n	DIFFOUT_B116n	AA8				
4A	VREFB4AN0	IO		DATA13	DIFFIO_TX_B116p	DIFFOUT_B116p	AB7	DQ11B	DQ5B		
4A	VREFB4AN0	IO		DATA7	DIFFIO_RX_B117n	DIFFOUT_B117n	AK5	DQSn11B/QK11B	DQ5B		
4A	VREFB4AN0	IO		DATA8	DIFFIO_RX_B117p	DIFFOUT_B117p	AK4	DQS11B/CQ11B/CQn11B/QKn11B	DQ5B		
4A	VREFB4AN0	IO		DATA14	DIFFIO_TX_B118n	DIFFOUT_B118n	AD7				
4A	VREFB4AN0	IO		DATA15	DIFFIO_TX_B118p	DIFFOUT_B118p	AE7	DQ11B	DQ5B		
4A	VREFB4AN0	IO		DATA9	DIFFIO_RX_B119n	DIFFOUT_B119n	AA6	DQ11B	DQ5B		
4A	VREFB4AN0	IO		CLKUSR	DIFFIO_RX_B119p	DIFFOUT_B119p	AB6	DQ11B	DQ5B		
4A	VREFB4AN0	IO	VREFB4AN0				AC6				
4A	VREFB4AN0	IO					AC7	DQ11B	DQ5B		
4A	VREFB4AN0	IO	CLK11n		DIFFIO_RX_B120n	DIFFOUT_B120n	AE6	DQ11B	DQ5B		
4A	VREFB4AN0	IO	CLK11p		DIFFIO_RX_B120p	DIFFOUT_B120p	AF6	DQ11B	DQ5B		
4A	VREFB4AN0	IO	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_B121n	DIFFOUT_B121n	AG5				
4A	VREFB4AN0	IO	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB0		DIFFIO_TX_B121p	DIFFOUT_B121p	AH5	DQ12B	DQ5B		
4A	VREFB4AN0	IO	FPLL_BR_CLKOUT3,FPLL_BR_FBn		DIFFIO_RX_B122n	DIFFOUT_B122n	AH4	DQ12B	DQ5B		
4A	VREFB4AN0	IO	FPLL_BR_CLKOUT2,FPLL_BR_FBp,FPLL_BR_FB1		DIFFIO_RX_B122p	DIFFOUT_B122p	AJ4	DQ12B	DQ5B		
4A	VREFB4AN0	IO			DIFFIO_TX_B123n	DIFFOUT_B123n	AD6				
4A	VREFB4AN0	IO			DIFFIO_TX_B123p	DIFFOUT_B123p	AE5	DQ12B	DQ5B		
4A	VREFB4AN0	IO	CLK10n		DIFFIO_RX_B124n	DIFFOUT_B124n	AJ3	DQSn12B/QK12B	DQSn5B/QK5B		
4A	VREFB4AN0	IO	CLK10p		DIFFIO_RX_B124p	DIFFOUT_B124p	AK3	DQS12B/CQ12B/CQn12B/QKn12B	DQS5B/CQ5B/CQn5B/QKn5B		
4A	VREFB4AN0	IO			DIFFIO_TX_B125n	DIFFOUT_B125n	AG4				
4A	VREFB4AN0	IO			DIFFIO_TX_B125p	DIFFOUT_B125p	AG3	DQ12B	DQ5B		
4A	VREFB4AN0	IO	CLK9n		DIFFIO_RX_B126n	DIFFOUT_B126n	AJ1	DQ12B	DQ5B		
4A	VREFB4AN0	IO	CLK9p		DIFFIO_RX_B126p	DIFFOUT_B126p	AK2	DQ12B	DQ5B		
4A	VREFB4AN0	IO			DIFFIO_TX_B127n	DIFFOUT_B127n	AE4				
4A	VREFB4AN0	IO	RZQ_1		DIFFIO_TX_B127p	DIFFOUT_B127p	AF4	DQ12B	DQ5B		
4A	VREFB4AN0	IO	CLK8n		DIFFIO_RX_B128n	DIFFOUT_B128n	AH2	DQ12B	DQ5B		
4A	VREFB4AN0	IO	CLK8p		DIFFIO_RX_B128p	DIFFOUT_B128p	AH1	DQ12B	DQ5B		
		RREF_BR					AF1				
		DNU					AF2				
		DNU					AG2				
GXB_R0		REFCLK0Rp					W9				
GXB_R0		REFCLK0Rn					W8				
GXB_R0		GXB_RX_R0n,GXB_REFCLK_R0n					AD2*				
GXB_R0		GXB_RX_R0p,GXB_REFCLK_R0p					AD1*				
GXB_R0		GXB_TX_R0p					AC3*				
GXB_R0		GXB_TX_R0n					AC4*				
GXB_R0		GXB_RX_R1n,GXB_REFCLK_R1n					AB2				
GXB_R0		GXB_RX_R1p,GXB_REFCLK_R1p					AB1				
GXB_R0		GXB_TX_R1p					AA3				
GXB_R0		GXB_TX_R1n					AA4				
GXB_R0		GXB_RX_R2n,GXB_REFCLK_R2n					Y2				
GXB_R0		GXB_RX_R2p,GXB_REFCLK_R2p					Y1				
GXB_R0		GXB_TX_R2p					W3				
GXB_R0		GXB_TX_R2n					W4				
GXB_R1		REFCLK2Rp					U9				
GXB_R1		REFCLK2Rn					U8				
GXB_R1		GXB_RX_R6n,GXB_REFCLK_R6n					V2*				
GXB_R1		GXB_RX_R6p,GXB_REFCLK_R6p					V1*				
GXB_R1		GXB_TX_R6p					U3*				
GXB_R1		GXB_TX_R6n					U4*				
GXB_R1		GXB_RX_R7n,GXB_REFCLK_R7n					T2				
GXB_R1		GXB_RX_R7p,GXB_REFCLK_R7p					T1				
GXB_R1		GXB_TX_R7p					R3				
GXB_R1		GXB_TX_R7n					R4				
GXB_R1		GXB_RX_R8n,GXB_REFCLK_R8n					P2*				
GXB_R1		GXB_RX_R8p,GXB_REFCLK_R8p					P1*				
GXB_R1		GXB_TX_R8p					N3*				
GXB_R1		GXB_TX_R8n					N4*				

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896 *(3)*	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36	DDR3/DDR2 Hard Memory PHY *(4)*
GXB_R1		GXB_RX_R9n,GXB_REFCLK_R9n					M2*				
GXB_R1		GXB_RX_R9p,GXB_REFCLK_R9p					M1*				
GXB_R1		GXB_TX_R9p					L3*				
GXB_R1		GXB_TX_R9n					L4*				
GXB_R1		GXB_RX_R10n,GXB_REFCLK_R10n					K2				
GXB_R1		GXB_RX_R10p,GXB_REFCLK_R10p					K1				
GXB_R1		GXB_TX_R10p					J3				
GXB_R1		GXB_TX_R10n					J4				
GXB_R1		GXB_RX_R11n,GXB_REFCLK_R11n					H2*				
GXB_R1		GXB_RX_R11p,GXB_REFCLK_R11p					H1*				
GXB_R1		GXB_TX_R11p					G3*				
GXB_R1		GXB_TX_R11n					G4*				
GXB_R1		REFCLK3Rp					R9				
GXB_R1		REFCLK3Rn					R8				
		DNU					H5				
7A		GND					F5				
7A	VREFB7AN0	IO	CLK12p		DIFFIO_RX_T1p	DIFFOUT_T1p	E1	DQ1T	DQ1T		
7A	VREFB7AN0	IO	CLK12n		DIFFIO_RX_T1n	DIFFOUT_T1n	F1	DQ1T	DQ1T		
7A	VREFB7AN0	IO	RZQ_5		DIFFIO_TX_T2p	DIFFOUT_T2p	E4	DQ1T	DQ1T		
7A	VREFB7AN0	IO			DIFFIO_TX_T2n	DIFFOUT_T2n	E3				
7A	VREFB7AN0	IO	CLK13p		DIFFIO_RX_T3p	DIFFOUT_T3p	D2	DQ1T	DQ1T		
7A	VREFB7AN0	IO	CLK13n		DIFFIO_RX_T3n	DIFFOUT_T3n	D1	DQ1T	DQ1T		
7A	VREFB7AN0	IO			DIFFIO_TX_T4p	DIFFOUT_T4p	D4	DQ1T	DQ1T		
7A	VREFB7AN0	IO			DIFFIO_TX_T4n	DIFFOUT_T4n	D3				
7A	VREFB7AN0	IO	CLK14p		DIFFIO_RX_T5p	DIFFOUT_T5p	A2	DQS1T/CQ1T/CQn1T/QKn1T	DQS1T/CQ1T/CQn1T/QKn1T		
7A	VREFB7AN0	IO	CLK14n		DIFFIO_RX_T5n	DIFFOUT_T5n	B1	DQSn1T/QK1T	DQSn1T/QK1T		
7A	VREFB7AN0	IO			DIFFIO_TX_T6p	DIFFOUT_T6p	C2	DQ1T	DQ1T		
7A	VREFB7AN0	IO			DIFFIO_TX_T6n	DIFFOUT_T6n	C1				
7A	VREFB7AN0	IO	FPLL_TR_CLKOUT2,FPLL_TR_FBp,FPLL_TR_FB1		DIFFIO_RX_T7p	DIFFOUT_T7p	A3	DQ1T	DQ1T		
7A	VREFB7AN0	IO	FPLL_TR_CLKOUT3,FPLL_TR_FBn		DIFFIO_RX_T7n	DIFFOUT_T7n	B3	DQ1T	DQ1T		
7A	VREFB7AN0	IO	FPLL_TR_CLKOUT0,FPLL_TR_CLKOUTp,FPLL_TR_FB0		DIFFIO_TX_T8p	DIFFOUT_T8p	B4	DQ1T	DQ1T		
7A	VREFB7AN0	IO	FPLL_TR_CLKOUT1,FPLL_TR_CLKOUTn		DIFFIO_TX_T8n	DIFFOUT_T8n	C4				
7A	VREFB7AN0	IO	CLK15p		DIFFIO_RX_T9p	DIFFOUT_T9p	C5	DQ2T	DQ1T		
7A	VREFB7AN0	IO	CLK15n		DIFFIO_RX_T9n	DIFFOUT_T9n	D5	DQ2T	DQ1T		
7A	VREFB7AN0	IO					J6	DQ2T	DQ1T		
7A	VREFB7AN0	IO	VREFB7AN0				K6				
7A	VREFB7AN0	IO		DEV_OE	DIFFIO_RX_T10p	DIFFOUT_T10p	A5	DQ2T	DQ1T		
7A	VREFB7AN0	IO		DEV_CLRn	DIFFIO_RX_T10n	DIFFOUT_T10n	A4	DQ2T	DQ1T		
7A	VREFB7AN0	IO			DIFFIO_TX_T11p	DIFFOUT_T11p	J7	DQ2T	DQ1T		
7A	VREFB7AN0	IO		nPERSTL0	DIFFIO_TX_T11n	DIFFOUT_T11n	K7				
7A	VREFB7AN0	IO		CvP_CONFDONE	DIFFIO_RX_T12p	DIFFOUT_T12p	D6	DQS2T/CQ2T/CQn2T/QKn2T	DQ1T		
7A	VREFB7AN0	IO		CRC_ERROR	DIFFIO_RX_T12n	DIFFOUT_T12n	E6	DQSn2T/QK2T	DQ1T		
7A	VREFB7AN0	IO		PR_DONE	DIFFIO_TX_T13p	DIFFOUT_T13p	G6	DQ2T	DQ1T		
7A	VREFB7AN0	IO		PR_REQUEST	DIFFIO_TX_T13n	DIFFOUT_T13n	H6				
7A	VREFB7AN0	IO		INIT_DONE	DIFFIO_RX_T14p	DIFFOUT_T14p	A6	DQ2T	DQ1T		
7A	VREFB7AN0	IO		nCEO	DIFFIO_RX_T14n	DIFFOUT_T14n	B6	DQ2T	DQ1T		
7A	VREFB7AN0	IO		PR_ERROR	DIFFIO_TX_T15p	DIFFOUT_T15p	G7	DQ2T	DQ1T		
7A	VREFB7AN0	IO		PR_READY	DIFFIO_TX_T15n	DIFFOUT_T15n	H7				
7B	VREFB7BN0	IO			DIFFIO_RX_T16p	DIFFOUT_T16p	F8	DQ3T	DQ2T	DQ1T	DQ4_7B_0
7B	VREFB7BN0	IO			DIFFIO_RX_T16n	DIFFOUT_T16n	G8	DQ3T	DQ2T	DQ1T	DQ4_7B_1
7B	VREFB7BN0	IO					J8	DQ3T	DQ2T	DQ1T	DQ4_7B_2
7B	VREFB7BN0	IO	VREFB7BN0				K8				
7B	VREFB7BN0	IO			DIFFIO_RX_T17p	DIFFOUT_T17p	E7	DQ3T	DQ2T	DQ1T	DQ4_7B_3
7B	VREFB7BN0	IO			DIFFIO_RX_T17n	DIFFOUT_T17n	F7	DQ3T	DQ2T	DQ1T	DQ4_7B_4
7B	VREFB7BN0	IO			DIFFIO_TX_T18p	DIFFOUT_T18p	G9	DQ3T	DQ2T	DQ1T	DQ4_7B_5
7B	VREFB7BN0	IO			DIFFIO_TX_T18n	DIFFOUT_T18n	H9				
7B	VREFB7BN0	IO			DIFFIO_RX_T19p	DIFFOUT_T19p	A7	DQS3T/CQ3T/CQn3T/QKn3T	DQS2T/CQ2T/CQn2T/QKn2T	DQ1T	DQS4_7B
7B	VREFB7BN0	IO			DIFFIO_RX_T19n	DIFFOUT_T19n	A8	DQSn3T/QK3T	DQSn2T/QK2T	DQ1T	DQS#4_7B
7B	VREFB7BN0	IO			DIFFIO_TX_T20p	DIFFOUT_T20p	B7	DQ3T	DQ2T	DQ1T	DM4_7B
7B	VREFB7BN0	IO			DIFFIO_TX_T20n	DIFFOUT_T20n	C7				
7B	VREFB7BN0	IO			DIFFIO_RX_T21p	DIFFOUT_T21p	C8	DQ3T	DQ2T	DQ1T	DQ4_7B_6
7B	VREFB7BN0	IO			DIFFIO_RX_T21n	DIFFOUT_T21n	D8	DQ3T	DQ2T	DQ1T	DQ4_7B_7
7B	VREFB7BN0	IO			DIFFIO_TX_T22p	DIFFOUT_T22p	J9	DQ3T	DQ2T	DQ1T	DQ4_7B_8
7B	VREFB7BN0	IO			DIFFIO_TX_T22n	DIFFOUT_T22n	K9				
7B	VREFB7BN0	IO			DIFFIO_RX_T23p	DIFFOUT_T23p	D9	DQ4T	DQ2T	DQ1T	DQ3_7B_0
7B	VREFB7BN0	IO			DIFFIO_RX_T23n	DIFFOUT_T23n	E9	DQ4T	DQ2T	DQ1T	DQ3_7B_1
7B	VREFB7BN0	IO			DIFFIO_TX_T24p	DIFFOUT_T24p	B10	DQ4T	DQ2T	DQ1T	DQ3_7B_2
7B	VREFB7BN0	IO			DIFFIO_TX_T24n	DIFFOUT_T24n	B9				
7B	VREFB7BN0	IO			DIFFIO_RX_T25p	DIFFOUT_T25p	A11	DQ4T	DQ2T	DQ1T	DQ3_7B_3
7B	VREFB7BN0	IO			DIFFIO_RX_T25n	DIFFOUT_T25n	A10	DQ4T	DQ2T	DQ1T	DQ3_7B_4
7B	VREFB7BN0	IO			DIFFIO_TX_T26p	DIFFOUT_T26p	J10	DQ4T	DQ2T	DQ1T	DQ3_7B_5
7B	VREFB7BN0	IO			DIFFIO_TX_T26n	DIFFOUT_T26n	K10				
7B	VREFB7BN0	IO			DIFFIO_RX_T27p	DIFFOUT_T27p	C10	DQS4T/CQ4T/CQn4T/QKn4T	DQ2T	DQS1T/CQ1T/CQn1T/QKn1T	DQS3_7B
7B	VREFB7BN0	IO			DIFFIO_RX_T27n	DIFFOUT_T27n	D10	DQSn4T/QK4T	DQ2T	DQSn1T/QK1T	DQS#3_7B
7B	VREFB7BN0	IO			DIFFIO_TX_T28p	DIFFOUT_T28p	E10	DQ4T	DQ2T	DQ1T	DM3_7B
7B	VREFB7BN0	IO			DIFFIO_TX_T28n	DIFFOUT_T28n	F10				
7B	VREFB7BN0	IO			DIFFIO_RX_T29p	DIFFOUT_T29p	C11	DQ4T	DQ2T	DQ1T	DQ3_7B_6
7B	VREFB7BN0	IO			DIFFIO_RX_T29n	DIFFOUT_T29n	D11	DQ4T	DQ2T	DQ1T	DQ3_7B_7
7B	VREFB7BN0	IO			DIFFIO_TX_T30p	DIFFOUT_T30p	G10	DQ4T	DQ2T	DQ1T	DQ3_7B_8
7B	VREFB7BN0	IO			DIFFIO_TX_T30n	DIFFOUT_T30n	H10				
7C	VREFB7CN0	IO			DIFFIO_RX_T31p	DIFFOUT_T31p	J11	DQ5T	DQ3T	DQ1T	DQ2_7C_0
7C	VREFB7CN0	IO			DIFFIO_RX_T31n	DIFFOUT_T31n	K11	DQ5T	DQ3T	DQ1T	DQ2_7C_1
7C	VREFB7CN0	IO			DIFFIO_TX_T32p	DIFFOUT_T32p	F11	DQ5T	DQ3T	DQ1T	DQ2_7C_2
7C	VREFB7CN0	IO			DIFFIO_TX_T32n	DIFFOUT_T32n	G11				
7C	VREFB7CN0	IO			DIFFIO_RX_T33p	DIFFOUT_T33p	B13	DQ5T	DQ3T	DQ1T	DQ2_7C_3
7C	VREFB7CN0	IO			DIFFIO_RX_T33n	DIFFOUT_T33n	B12	DQ5T	DQ3T	DQ1T	DQ2_7C_4
7C	VREFB7CN0	IO			DIFFIO_TX_T34p	DIFFOUT_T34p	D12	DQ5T	DQ3T	DQ1T	DQ2_7C_5
7C	VREFB7CN0	IO			DIFFIO_TX_T34n	DIFFOUT_T34n	E12				
7C	VREFB7CN0	IO			DIFFIO_RX_T35p	DIFFOUT_T35p	J12	DQS5T/CQ5T/CQn5T/QKn5T	DQS3T/CQ3T/CQn3T/QKn3T	DQ1T	DQS2_7C
7C	VREFB7CN0	IO			DIFFIO_RX_T35n	DIFFOUT_T35n	K12	DQSn5T/QK5T	DQSn3T/QK3T	DQ1T	DQS#2_7C
7C	VREFB7CN0	IO			DIFFIO_TX_T36p	DIFFOUT_T36p	G12	DQ5T	DQ3T	DQ1T	DM2_7C
7C	VREFB7CN0	IO			DIFFIO_TX_T36n	DIFFOUT_T36n	H12				
7C	VREFB7CN0	IO			DIFFIO_RX_T37p	DIFFOUT_T37p	C13	DQ5T	DQ3T	DQ1T	DQ2_7C_6
7C	VREFB7CN0	IO			DIFFIO_RX_T37n	DIFFOUT_T37n	D13	DQ5T	DQ3T	DQ1T	DQ2_7C_7

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896 *(3)*	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36	DDR3/DDR2 Hard Memory PHY *(4)*
7C	VREFB7CN0	IO			DIFFIO_TX_T38p	DIFFOUT_T38p	E13	DQ5T	DQ3T	DQ1T	DQ2_7C_8
7C	VREFB7CN0	IO			DIFFIO_TX_T38n	DIFFOUT_T38n	F13				
7C	VREFB7CN0	IO			DIFFIO_RX_T39p	DIFFOUT_T39p	J14	DQ6T	DQ3T	DQ1T	DQ1_7C_0
7C	VREFB7CN0	IO			DIFFIO_RX_T39n	DIFFOUT_T39n	K14	DQ6T	DQ3T	DQ1T	DQ1_7C_1
7C	VREFB7CN0	IO					J13	DQ6T	DQ3T	DQ1T	DQ1_7C_2
7C	VREFB7CN0	IO	VREFB7CN0				K13				
7C	VREFB7CN0	IO			DIFFIO_RX_T40p	DIFFOUT_T40p	A14	DQ6T	DQ3T	DQ1T	DQ1_7C_3
7C	VREFB7CN0	IO			DIFFIO_RX_T40n	DIFFOUT_T40n	A13	DQ6T	DQ3T	DQ1T	DQ1_7C_4
7C	VREFB7CN0	IO			DIFFIO_TX_T41p	DIFFOUT_T41p	F14	DQ6T	DQ3T	DQ1T	DQ1_7C_5
7C	VREFB7CN0	IO			DIFFIO_TX_T41n	DIFFOUT_T41n	G14				
7C	VREFB7CN0	IO			DIFFIO_RX_T42p	DIFFOUT_T42p	C14	DQS6T/CQ6T/CQn6T/QKn6T	DQ3T	DQ1T	DQS1_7C
7C	VREFB7CN0	IO			DIFFIO_RX_T42n	DIFFOUT_T42n	D14	DQSn6T/QK6T	DQ3T	DQ1T	DQS#1_7C
7C	VREFB7CN0	IO			DIFFIO_TX_T43p	DIFFOUT_T43p	G13	DQ6T	DQ3T	DQ1T	DM1_7C
7C	VREFB7CN0	IO			DIFFIO_TX_T43n	DIFFOUT_T43n	H13				
7C	VREFB7CN0	IO			DIFFIO_RX_T44p	DIFFOUT_T44p	A15	DQ6T	DQ3T	DQ1T	DQ1_7C_6
7C	VREFB7CN0	IO			DIFFIO_RX_T44n	DIFFOUT_T44n	B15	DQ6T	DQ3T	DQ1T	DQ1_7C_7
7C	VREFB7CN0	IO			DIFFIO_TX_T45p	DIFFOUT_T45p	D15	DQ6T	DQ3T	DQ1T	DQ1_7C_8
7C	VREFB7CN0	IO			DIFFIO_TX_T45n	DIFFOUT_T45n	E15				RESET#_7D
7D	VREFB7DN0	IO			DIFFIO_RX_T46p	DIFFOUT_T46p	F15	DQ7T	DQ4T		CK_7D
7D	VREFB7DN0	IO			DIFFIO_RX_T46n	DIFFOUT_T46n	G15	DQ7T	DQ4T		CK#_7D
7D	VREFB7DN0	IO			DIFFIO_TX_T47p	DIFFOUT_T47p	J16	DQ7T	DQ4T		CKE_7D_0
7D	VREFB7DN0	IO			DIFFIO_TX_T47n	DIFFOUT_T47n	K16				CKE_7D_1
7D	VREFB7DN0	IO			DIFFIO_RX_T48p	DIFFOUT_T48p	H15	DQ7T	DQ4T		A_7D_0
7D	VREFB7DN0	IO			DIFFIO_RX_T48n	DIFFOUT_T48n	J15	DQ7T	DQ4T		A_7D_1
7D	VREFB7DN0	IO			DIFFIO_TX_T49p	DIFFOUT_T49p	D16	DQ7T	DQ4T		A_7D_2
7D	VREFB7DN0	IO			DIFFIO_TX_T49n	DIFFOUT_T49n	E16				A_7D_3
7D	VREFB7DN0	IO			DIFFIO_RX_T50p	DIFFOUT_T50p	B16	DQS7T/CQ7T/CQn7T/QKn7T	DQS4T/CQ4T/CQn4T/QKn4T		A_7D_4
7D	VREFB7DN0	IO			DIFFIO_RX_T50n	DIFFOUT_T50n	C16	DQSn7T/QK7T	DQSn4T/QK4T		A_7D_5
7D	VREFB7DN0	IO			DIFFIO_TX_T51p	DIFFOUT_T51p	G16	DQ7T	DQ4T		A_7D_6
7D	VREFB7DN0	IO			DIFFIO_TX_T51n	DIFFOUT_T51n	H16				A_7D_7
7D	VREFB7DN0	IO			DIFFIO_RX_T52p	DIFFOUT_T52p	A17	DQ7T	DQ4T		A_7D_8
7D	VREFB7DN0	IO			DIFFIO_RX_T52n	DIFFOUT_T52n	A16	DQ7T	DQ4T		A_7D_9
7D	VREFB7DN0	IO			DIFFIO_TX_T53p	DIFFOUT_T53p	C17	DQ7T	DQ4T		A_7D_10
7D	VREFB7DN0	IO			DIFFIO_TX_T53n	DIFFOUT_T53n	D17				A_7D_11
7D	VREFB7DN0	IO			DIFFIO_RX_T54p	DIFFOUT_T54p	J17	DQ8T	DQ4T		A_7D_12
7D	VREFB7DN0	IO			DIFFIO_RX_T54n	DIFFOUT_T54n	K17	DQ8T	DQ4T		A_7D_13
7D	VREFB7DN0	IO					J18	DQ8T	DQ4T		A_7D_14
7D	VREFB7DN0	IO	VREFB7DN0				K18				
7D	VREFB7DN0	IO			DIFFIO_RX_T55p	DIFFOUT_T55p	D18	DQ8T	DQ4T		BA_7D_0
7D	VREFB7DN0	IO			DIFFIO_RX_T55n	DIFFOUT_T55n	E18	DQ8T	DQ4T		BA_7D_1
7D	VREFB7DN0	IO			DIFFIO_TX_T56p	DIFFOUT_T56p	F17	DQ8T	DQ4T		BA_7D_2
7D	VREFB7DN0	IO			DIFFIO_TX_T56n	DIFFOUT_T56n	G17				RAS#_7D
7D	VREFB7DN0	IO			DIFFIO_RX_T57p	DIFFOUT_T57p	B18	DQS8T/CQ8T/CQn8T/QKn8T	DQ4T		CAS#_7D
7D	VREFB7DN0	IO			DIFFIO_RX_T57n	DIFFOUT_T57n	C19	DQSn8T/QK8T	DQ4T		WE#_7D
7D	VREFB7DN0	IO			DIFFIO_TX_T58p	DIFFOUT_T58p	G18	DQ8T	DQ4T		ODT_7D_0
7D	VREFB7DN0	IO			DIFFIO_TX_T58n	DIFFOUT_T58n	H18				ODT_7D_1
7D	VREFB7DN0	IO			DIFFIO_RX_T59p	DIFFOUT_T59p	A19	DQ8T	DQ4T		A_7D_15
7D	VREFB7DN0	IO			DIFFIO_RX_T59n	DIFFOUT_T59n	B19	DQ8T	DQ4T		
7D	VREFB7DN0	IO			DIFFIO_TX_T60p	DIFFOUT_T60p	D19	DQ8T	DQ4T		CS#_7D_0
7D	VREFB7DN0	IO			DIFFIO_TX_T60n	DIFFOUT_T60n	E19				CS#_7D_1
		VCCA_FPLL					M16				
		VCCD_FPLL					M15				
		DNU					K15				
8D	VREFB8DN0	IO	CLK19p		DIFFIO_RX_T61p	DIFFOUT_T61p	F19	DQ9T	DQ5T		
8D	VREFB8DN0	IO	CLK19n		DIFFIO_RX_T61n	DIFFOUT_T61n	G20	DQ9T	DQ5T		
8D	VREFB8DN0	IO			DIFFIO_TX_T62p	DIFFOUT_T62p	J19	DQ9T	DQ5T		
8D	VREFB8DN0	IO			DIFFIO_TX_T62n	DIFFOUT_T62n	K19				
8D	VREFB8DN0	IO	CLK18p		DIFFIO_RX_T63p	DIFFOUT_T63p	J20	DQ9T	DQ5T		
8D	VREFB8DN0	IO	CLK18n		DIFFIO_RX_T63n	DIFFOUT_T63n	K20	DQ9T	DQ5T		
8D	VREFB8DN0	IO			DIFFIO_TX_T64p	DIFFOUT_T64p	F20	DQ9T	DQ5T		
8D	VREFB8DN0	IO			DIFFIO_TX_T64n	DIFFOUT_T64n	F21				
8D	VREFB8DN0	IO	FPLL_TC_CLKOUT2,FPLL_TC_FBp,FPLL_TC_FB1		DIFFIO_RX_T65p	DIFFOUT_T65p	C20	DQS9T/CQ9T/CQn9T/QKn9T	DQS5T/CQ5T/CQn5T/QKn5T		
8D	VREFB8DN0	IO	FPLL_TC_CLKOUT3,FPLL_TC_FBn		DIFFIO_RX_T65n	DIFFOUT_T65n	D20	DQSn9T/QK9T	DQSn5T/QK5T		
8D	VREFB8DN0	IO	FPLL_TC_CLKOUT0,FPLL_TC_CLKOUTp,FPLL_TC_FB0		DIFFIO_TX_T66p	DIFFOUT_T66p	G19	DQ9T	DQ5T		
8D	VREFB8DN0	IO	FPLL_TC_CLKOUT1,FPLL_TC_CLKOUTn		DIFFIO_TX_T66n	DIFFOUT_T66n	H19				
8D	VREFB8DN0	IO	CLK17p		DIFFIO_RX_T67p	DIFFOUT_T67p	A21	DQ9T	DQ5T		
8D	VREFB8DN0	IO	CLK17n		DIFFIO_RX_T67n	DIFFOUT_T67n	B21	DQ9T	DQ5T		
8D	VREFB8DN0	IO			DIFFIO_TX_T68p	DIFFOUT_T68p	D21	DQ9T	DQ5T		
8D	VREFB8DN0	IO			DIFFIO_TX_T68n	DIFFOUT_T68n	E21				
8D	VREFB8DN0	IO	CLK16p		DIFFIO_RX_T69p	DIFFOUT_T69p	D22	DQ10T	DQ5T		
8D	VREFB8DN0	IO	CLK16n		DIFFIO_RX_T69n	DIFFOUT_T69n	E22	DQ10T	DQ5T		
8D	VREFB8DN0	IO					J21	DQ10T	DQ5T		
8D	VREFB8DN0	IO	VREFB8DN0				K21				
8D	VREFB8DN0	IO			DIFFIO_RX_T70p	DIFFOUT_T70p	J22	DQ10T	DQ5T		
8D	VREFB8DN0	IO			DIFFIO_RX_T70n	DIFFOUT_T70n	K22	DQ10T	DQ5T		
8D	VREFB8DN0	IO			DIFFIO_TX_T71p	DIFFOUT_T71p	G22	DQ10T	DQ5T		
8D	VREFB8DN0	IO			DIFFIO_TX_T71n	DIFFOUT_T71n	H22				
8D	VREFB8DN0	IO			DIFFIO_RX_T72p	DIFFOUT_T72p	B22	DQS10T/CQ10T/CQn10T/QKn10T	DQ5T		
8D	VREFB8DN0	IO			DIFFIO_RX_T72n	DIFFOUT_T72n	C22	DQSn10T/QK10T	DQ5T		
8D	VREFB8DN0	IO			DIFFIO_TX_T73p	DIFFOUT_T73p	G21	DQ10T	DQ5T		
8D	VREFB8DN0	IO			DIFFIO_TX_T73n	DIFFOUT_T73n	H21				
8D	VREFB8DN0	IO			DIFFIO_RX_T74p	DIFFOUT_T74p	F23	DQ10T	DQ5T		
8D	VREFB8DN0	IO			DIFFIO_RX_T74n	DIFFOUT_T74n	G23	DQ10T	DQ5T		
8D	VREFB8DN0	IO			DIFFIO_TX_T75p	DIFFOUT_T75p	C23	DQ10T	DQ5T		
8D	VREFB8DN0	IO			DIFFIO_TX_T75n	DIFFOUT_T75n	D23				
8A	VREFB8AN0	IO			DIFFIO_RX_T114p	DIFFOUT_T114p	A23	DQ11T			
8A	VREFB8AN0	IO			DIFFIO_RX_T114n	DIFFOUT_T114n	A24	DQ11T			
8A	VREFB8AN0	IO			DIFFIO_TX_T115p	DIFFOUT_T115p	L22	DQ11T			
8A	VREFB8AN0	IO			DIFFIO_TX_T115n	DIFFOUT_T115n	K23				
8A	VREFB8AN0	IO			DIFFIO_RX_T116p	DIFFOUT_T116p	D24	DQ11T			
8A	VREFB8AN0	IO			DIFFIO_RX_T116n	DIFFOUT_T116n	E24	DQ11T			
8A	VREFB8AN0	IO			DIFFIO_TX_T117p	DIFFOUT_T117p	B24	DQ11T			
8A	VREFB8AN0	IO			DIFFIO_TX_T117n	DIFFOUT_T117n	B25				
8A	VREFB8AN0	IO			DIFFIO_RX_T118p	DIFFOUT_T118p	A26	DQS11T/CQ11T/CQn11T/QKn11T			

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896 *(3)*	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36	DDR3/DDR2 Hard Memory PHY *(4)*
8A	VREFB8AN0	IO			DIFFIO_RX_T118n	DIFFOUT_T118n	A27	DQSn11T/QK11T			
8A	VREFB8AN0	IO			DIFFIO_TX_T119p	DIFFOUT_T119p	K24	DQ11T			
8A	VREFB8AN0	IO			DIFFIO_TX_T119n	DIFFOUT_T119n	J23				
8A	VREFB8AN0	IO	CLK23p		DIFFIO_RX_T120p	DIFFOUT_T120p	C25	DQ11T			
8A	VREFB8AN0	IO	CLK23n		DIFFIO_RX_T120n	DIFFOUT_T120n	D25	DQ11T			
8A	VREFB8AN0	IO			DIFFIO_TX_T121p	DIFFOUT_T121p	J25	DQ11T			
8A	VREFB8AN0	IO			DIFFIO_TX_T121n	DIFFOUT_T121n	K25				
8A	VREFB8AN0	IO	CLK22p		DIFFIO_RX_T122p	DIFFOUT_T122p	D26	DQ12T			
8A	VREFB8AN0	IO	CLK22n		DIFFIO_RX_T122n	DIFFOUT_T122n	E25	DQ12T			
8A	VREFB8AN0	IO					G24	DQ12T			
8A	VREFB8AN0	IO	VREFB8AN0				H25				
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT2,FPLL_TL_FBp,FPLL_TL_FB1		DIFFIO_RX_T123p	DIFFOUT_T123p	C27	DQ12T			
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT3,FPLL_TL_FBn		DIFFIO_RX_T123n	DIFFOUT_T123n	C26	DQ12T			
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB0		DIFFIO_TX_T124p	DIFFOUT_T124p	A28	DQ12T			
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T124n	DIFFOUT_T124n	B27				
8A	VREFB8AN0	IO	CLK21p		DIFFIO_RX_T125p	DIFFOUT_T125p	A29	DQS12T/CQ12T/CQn12T/QKn12T			
8A	VREFB8AN0	IO	CLK21n		DIFFIO_RX_T125n	DIFFOUT_T125n	B28	DQSn12T/QK12T			
8A	VREFB8AN0	IO			DIFFIO_TX_T126p	DIFFOUT_T126p	H24	DQ12T			
8A	VREFB8AN0	IO			DIFFIO_TX_T126n	DIFFOUT_T126n	J24				
8A	VREFB8AN0	IO	CLK20p		DIFFIO_RX_T127p	DIFFOUT_T127p	C28	DQ12T			
8A	VREFB8AN0	IO	CLK20n		DIFFIO_RX_T127n	DIFFOUT_T127n	D27	DQ12T			
8A	VREFB8AN0	IO			DIFFIO_TX_T128p	DIFFOUT_T128p	F25	DQ12T			
8A	VREFB8AN0	IO	RZQ_6		DIFFIO_TX_T128n	DIFFOUT_T128n	G25				
8A		MSEL0		MSEL0			C30				
8A		MSEL1		MSEL1			D30				
8A		MSEL2		MSEL2			C29				
8A		MSEL3		MSEL3			D29				
8A		MSEL4		MSEL4			F26				
8A		CONF_DONE		CONF_DONE			B30				
8A		nSTATUS		nSTATUS			D28				
8A		nCE		nCE			E28				
8A		nCONFIG		nCONFIG			E27				
8A		GND					H26				
		GND					AA26				
		GND					AA29				
		GND					AA30				
		GND					AB27				
		GND					AB28				
		GND					AC26				
		GND					AC29				
		GND					AC30				
		GND					AD27				
		GND					AD28				
		GND					AE28				
		GND					AE29				
		GND					AE30				
		GND					E30				
		GND					F27				
		GND					F28				
		GND					G26				
		GND					G29				
		GND					G30				
		GND					H27				
		GND					H28				
		GND					J26				
		GND					J29				
		GND					J30				
		GND					K27				
		GND					K28				
		GND					L25				
		GND					L26				
		GND					L29				
		GND					L30				
		GND					M24				
		GND					M27				
		GND					M28				
		GND					N23				
		GND					N24				
		GND					N26				
		GND					N29				
		GND					N30				
		GND					P23				
		GND					P25				
		GND					P27				
		GND					P28				
		GND					R24				
		GND					R29				
		GND					R30				
		GND					T23				
		GND					T27				
		GND					T28				
		GND					U24				
		GND					U26				
		GND					U29				
		GND					U30				
		GND					V23				
		GND					V25				
		GND					V27				
		GND					V28				
		GND					W24				
		GND					W29				
		GND					W30				
		GND					Y22				
		GND					Y23				

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896 *(3)*	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36	DDR3/DDR2 Hard Memory PHY *(4)*
		GND					Y24				
		GND					Y25				
		GND					Y26				
		GND					Y27				
		GND					Y28				
		GND					AA1				
		GND					AA2				
		GND					AA5				
		GND					AB3				
		GND					AB4				
		GND					AC1				
		GND					AC2				
		GND					AC5				
		GND					AD3				
		GND					AD4				
		GND					AE1				
		GND					AE2				
		GND					AE3				
		GND					AG1				
		GND					F3				
		GND					F4				
		GND					G1				
		GND					G2				
		GND					G5				
		GND					H3				
		GND					H4				
		GND					J1				
		GND					J2				
		GND					J5				
		GND					K3				
		GND					K4				
		GND					L1				
		GND					L2				
		GND					L5				
		GND					L6				
		GND					M3				
		GND					M4				
		GND					M7				
		GND					N1				
		GND					N2				
		GND					N5				
		GND					N8				
		GND					N9				
		GND					P3				
		GND					P4				
		GND					P6				
		GND					P8				
		GND					R1				
		GND					R2				
		GND					R5				
		GND					R7				
		GND					T3				
		GND					T4				
		GND					T8				
		GND					U1				
		GND					U2				
		GND					U5				
		GND					U7				
		GND					V3				
		GND					V4				
		GND					V6				
		GND					V8				
		GND					W1				
		GND					W2				
		GND					W7				
		GND					Y3				
		GND					Y4				
		GND					Y5				
		GND					Y6				
		GND					Y7				
		GND					Y8				
		GND					Y9				
		VCCP					L11				
		VCCP					L15				
		VCCP					L19				
		VCCP					L20				
		VCCP					L9				
		VCCP					W11				
		VCCP					W13				
		VCCP					W17				
		VCCP					W19				
		VCCP					W21				
		VCCA_FPLL					T22				
		VCCA_FPLL					T9				
		VCCA_FPLL					P22				
		VCCA_FPLL					P9				
		VCCBAT					K26				
		VCC_AUX					M12				
		VCC_AUX					M18				
		VCC_AUX					W12				
		VCC_AUX					W18				
		VCCD_FPLL					V22				
		VCCD_FPLL					V9				
		VCCD_FPLL					N22				

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896 *(3)*	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36	DDR3/DDR2 Hard Memory PHY *(4)*
		VCCD_FPLL					M8				
		VCCA_GXBL0					V24				
		VCCA_GXBR0					V7				
		VCCA_GXBL1					P24				
		VCCA_GXBR1					P7				
		VCCH_GXBL0					T24				
		VCCH_GXBR0					T7				
		VCCH_GXBL1					N25				
		VCCH_GXBR1					N7				
		VCCL_GXBL0					T25				
		VCCL_GXBL0					T26				
		VCCL_GXBR0					U6				
		VCCL_GXBL1					M25				
		VCCL_GXBR1					M6				
		VCCL_GXBR1					N6				
		VCCR_GXBL					M26				
		VCCR_GXBL					R25				
		VCCR_GXBL					R26				
		VCCR_GXBL					W25				
		VCCR_GXBL					W26				
		VCCR_GXBR					M5				
		VCCR_GXBR					T5				
		VCCR_GXBR					T6				
		VCCR_GXBR					W5				
		VCCR_GXBR					W6				
		VCCT_GXBL0					U25				
		VCCT_GXBL0					V26				
		VCCT_GXBR0					V5				
		VCCT_GXBL1					P26				
		VCCT_GXBR1					P5				
		VCCT_GXBR1					R6				
		VCC					M10				
		VCC					M14				
		VCC					M20				
		VCC					N11				
		VCC					N13				
		VCC					N15				
		VCC					N17				
		VCC					N19				
		VCC					N21				
		VCC					P10				
		VCC					P12				
		VCC					P14				
		VCC					P16				
		VCC					P18				
		VCC					P20				
		VCC					R11				
		VCC					R13				
		VCC					R15				
		VCC					R17				
		VCC					R19				
		VCC					R21				
		VCC					T10				
		VCC					T12				
		VCC					T14				
		VCC					T18				
		VCC					T20				
		VCC					U11				
		VCC					U13				
		VCC					U15				
		VCC					U17				
		VCC					U19				
		VCC					U21				
		VCC					V10				
		VCC					V12				
		VCC					V14				
		VCC					V16				
		VCC					V18				
		VCC					V20				
		VCC					T16				
		VCCIO3A					AD26				
		VCCIO3A					AE24				
		VCCIO3A					AH24				
		VCCIO3A					AH27				
		VCCIO3D					AE19				
		VCCIO3D					AE21				
		VCCIO3D					AH21				
		VCCIO3D					AK23				
		VCCIO4A					AB5				
		VCCIO4A					AD5				
		VCCIO4A					AH3				
		VCCIO4A					AH6				
		VCCIO4B					AE10				
		VCCIO4B					AG9				
		VCCIO4B					AH10				
		VCCIO4B					AK9				
		VCCIO4C					AE12				
		VCCIO4C					AG13				
		VCCIO4C					AK13				
		VCCIO4C					AK15				
		VCCIO4D					AE16				
		VCCIO4D					AG18				
		VCCIO4D					AH16				
		VCCIO4D					AK18				

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896 *(3)*	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36	DDR3/DDR2 Hard Memory PHY *(4)*
		VCCIO7A					C3				
		VCCIO7A					C6				
		VCCIO7A					F2				
		VCCIO7A					F6				
		VCCIO7B					A9				
		VCCIO7B					C9				
		VCCIO7B					D7				
		VCCIO7B					F9				
		VCCIO7C					A12				
		VCCIO7C					C12				
		VCCIO7C					C15				
		VCCIO7C					F12				
		VCCIO7D					A18				
		VCCIO7D					C18				
		VCCIO7D					F16				
		VCCIO7D					F18				
		VCCIO8A					A25				
		VCCIO8A					C24				
		VCCIO8A					F24				
		VCCIO8A					L23				
		VCCIO8D					A20				
		VCCIO8D					A22				
		VCCIO8D					C21				
		VCCIO8D					F22				
		VCCPD3					AA23				
		VCCPD3					Y21				
		VCCPD4A					AA7				
		VCCPD4BCD					Y10				
		VCCPD4BCD					Y15				
		VCCPD4BCD					Y18				
		VCCPD7A					L8				
		VCCPD7BCD					L13				
		VCCPD7BCD					L17				
		VCCPD7BCD					M9				
		VCCPD8					M22				
		VCCPD8					M23				
		VCCPGM					K5				
		VCCPGM					AA24				
		GND					AC11				
		GND					AC14				
		GND					AC17				
		GND					AC20				
		GND					AC23				
		GND					AC8				
		GND					AF11				
		GND					AF14				
		GND					AF17				
		GND					AF20				
		GND					AF23				
		GND					AF26				
		GND					AF3				
		GND					AF5				
		GND					AF8				
		GND					AH29				
		GND					AJ11				
		GND					AJ14				
		GND					AJ17				
		GND					AJ2				
		GND					AJ20				
		GND					AJ23				
		GND					AJ26				
		GND					AJ5				
		GND					AJ8				
		GND					B11				
		GND					B14				
		GND					B17				
		GND					B2				
		GND					B20				
		GND					B23				
		GND					B26				
		GND					B29				
		GND					B5				
		GND					B8				
		GND					E11				
		GND					E14				
		GND					E17				
		GND					E2				
		GND					E20				
		GND					E23				
		GND					E26				
		GND					E5				
		GND					E8				
		GND					H11				
		GND					H14				
		GND					H17				
		GND					H20				
		GND					H23				
		GND					H8				
		GND					L10				
		GND					L12				
		GND					L14				
		GND					L16				
		GND					L18				
		GND					L21				

Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896 *(3)*	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36	DDR3/DDR2 Hard Memory PHY *(4)*
		GND					L24				
		GND					L7				
		GND					M11				
		GND					M13				
		GND					M17				
		GND					M19				
		GND					M21				
		GND					N10				
		GND					N12				
		GND					N14				
		GND					N16				
		GND					N18				
		GND					N20				
		GND					P11				
		GND					P13				
		GND					P15				
		GND					P17				
		GND					P19				
		GND					P21				
		GND					R10				
		GND					R12				
		GND					R14				
		GND					R18				
		GND					R20				
		GND					T11				
		GND					T13				
		GND					T15				
		GND					T17				
		GND					T19				
		GND					T21				
		GND					U10				
		GND					U12				
		GND					U14				
		GND					U16				
		GND					U18				
		GND					U20				
		GND					V11				
		GND					V13				
		GND					V15				
		GND					V17				
		GND					V19				
		GND					V21				
		GND					W10				
		GND					W14				
		GND					W20				
		GND					Y11				
		GND					Y14				
		GND					Y17				
		GND					Y19				
		GND					R16				

Notes:
(1) For more information about pin definitions and pin connection guidelines, refer to the
Arria V Device Family Pin Connection Guidelines.
(2) The GXB_REFCLK pin is not supported in the current Quartus II version, but will be supported in the future Quartus II release version.
(3) Pins with * are with reference to the 10 Gbps transceiver channels. For more information about the 10 Gbps transceiver channels clocking recommendation, refer to the
Transceiver Clocking in Arria V Devices chapter.
(4) The RESET pin is only applicable for DDR3 devices.

Version Number	Date	Changes Made
1.0	1/30/2013	Initial release.
1.1	10/11/2013	- Removed F672 (Pin List DF27) and F1152 (Pin List GF35) packages. - Removed LPDDR2 hard memory PHY, RLDRAMII hard memory PHY, and QDRII hard memory PHY columns.