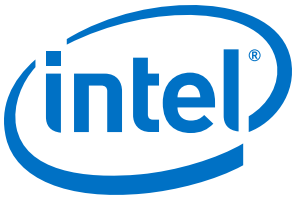

PCI Express: Migrating to Stratix 10 from Arria 10 for the Avalon-MM and Avalon-MM DMA Interfaces

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Contents

1 Introduction

This design migration reference guide describes differences in PCI Express implementations between the Arria® 10 (or Stratix® V) and Stratix 10 device families. It should ease migration from those earlier device families to Stratix 10 devices.

This guide covers the Avalon® Memory-Mapped (Avalon-MM) and Avalon-MM with DMA interfaces. A separate design migration reference guide covers the Avalon Streaming (Avalon-ST) interfaces.

2 Configuration Options

The parameters available to configure the PCI Express IP core in Stratix 10 devices differ from those available for Stratix V and Arria 10 devices. The following table describes the differences.

Table 1. Comparison of Stratix 10 and Stratix V or Arria 10 Parameters

Feature	Stratix 10	Stratix V or Arria 10	Comments
Supported Link Widths	1,2,4,8,16	1,2,4,8	
Interface widths	256 bits only	Avalon-MM: 64 or 128 bits Avalon-MM with DMA:128 or 256 bits	Stratix 10: Qsys automatically inserts width adaptation logic to interface to the user application.
Port type	Native Endpoint	Avalon-MM: Native Endpoint, Root Port Avalon-MM with DMA: Native Endpoint	Stratix 10 will support Root Ports in a future release.
Number of Avalon-MM slave interfaces supported	Supports the following 2 Avalon-MM TX slave interfaces for either Avalon-MM or Avalon-MM with DMA: • 256-bit high performance, bursting TX slave • 32-bit non-bursting TX slave	Supports a single Avalon-MM TX slave interface. Supported interfaces differ for Avalon-MM and Avalon-MM with DMA variants as follows: • Avalon-MM: 64-or 128-bit bursting interface • Avalon-MM with DMA: 32-bit non-bursting interface	
Avalon-MM and DMA support	The **Application interface type** parameter on the System Settings tab specifies Avalon-MM interface. The additional **Enable Avalon-MM DMA** parameter on the Avalon-MM Settings tab turns on the DMA capability.	The **Application interface type** parameter on the System Settings tab selects between **Avalon-MM** and **Avalon-MM with DMA** DMA interfaces.	Stratix 10: Up to 2 Avalon-MM interfaces with 1 implementing DMA. Arria 10, Stratix V: 1 Avalon-MM interface with or without DMA.
Interrupts	The **Export interrupt conduit interfaces** parameter on the Avalon-MM Settings tab exports interrupt interfaces.	The **Export MSI/MSI-X conduit interfaces** parameter on the Avalon-MM Settings tab exports interrupt interfaces.	Both parameters export MSI, MSI-X, and legacy interrupt interfaces.
Avalon-MM non-bursting slave interface	The **Enable non-bursting Avalon-MM Slave interface with individual byte access (TXS)** parameter on the Avalon-MM Settings tab controls Avalon-MM TX bursting slave support.	Non-bursting Avalon-MM TX slave port is always enabled.	Stratix 10: If DMA is enabled, the 32-bit non-bursting Avalon-MM slave interface must also be enabled. Arria 10, Stratix V: TX Avalon-MM slave port is always enabled.

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Feature	Stratix 10	Stratix V or Arria 10	Comments
Avalon-MM bursting interfaces	Bursting is available for all BARs. The **Enable burst capability for Avalon-MM BAR<*n*> Master port** on the Base Address Register tab turns on bursting.	When the **Application interface type** specifies the **Avalon-MM with DMA** interface, you can turn on **Enable burst capability for RXM BAR2 port** on the Avalon-MM Settings tab.	Arria 10, Stratix V: If BAR2 is 32-bits and burst capable, BAR3 is not available for other uses. If BAR2 is 64-bits and burst capable, BAR3 drives the upper 32 bits.
Tag support	256 tags.	32 tags. When the **Application Interface Type** is **Avalon-MM with DMA**, the Settings tab includes **Enable 256 tags** to enable additional tabs.	• For the Avalon-MM DMA interface, turning on **Enable 256 tags** improves the performance of high latency systems. This option turns on the `Extended Tag` bit in the `PCI Express Device Capabilities` Configuration Space register.
High performance Avalon-MM slave interface (HPTXS)	The **Enable High Performance bursting Avalon-MM Slave interface (HPTXS)** parameter on the Avalon-MM Settings tab turns this port on.	Not available.	Arria 10, Stratix V: No separate high performance Avalon-MM TX slave interface.
Address translation table size for high performance TX slave	2, 4, 8, 16, 32, 64, 128, 256, and 512 entries supported.	Separate high performance TX slave is not available.	
Error settings	By default, Advanced Error Reporting (AER), ECRC Checking, and ECRC Generation are on. You can turn off the AER capability in the `Advanced Error Reporting Extended Capability` register. You can turn off ECRC generation and checking in the `Advanced Error Capabilities and Control` register. The parameter editor does not provide controls for these settings.	You can configure the following error settings in the parameter editor. By default, they are all turned off. • AER • ECRC Generation • ECRC Checking	
CvP	Not supported in the current release.	The Configuration, Debug, and Extensions Options tab includes the **Enable Configuration via Protocol (CvP)** parameter.	Stratix 10: CvP will be supported in a future release.
Hard reset controller	Supports hard reset controller only.	Arria 10: supports hard reset controller only. Stratix V: hard reset controller for Gen1. Soft reset controller for Gen2 and Gen3.	
Design examples	Dynamically generated design example includes the parameters you specify.	Arria 10: Dynamically generated design example includes the parameters you specify. Stratix V: Static design examples are available in the installation directory.	

3 Interface and Signal Differences

3.1 Reset Interfaces

Table 2. Reset Interfaces

Stratix 10	Arria 10, Stratix V	Comments
app_nreset_status reset_status	nreset_status	Stratix 10: Supports two signals that have the same functionality but are polarity-inverted: • app_nreset_status an active-low reset • reset_status active high reset Arria 10, Stratix V: Supports only nreset_status, an active-low reset.

3.2 Serial Interface

Table 3. Serial Interface

Stratix 10	Arria 10, Stratix V	Comments
tx_out[<*n-1*>:0]	tx_out[<*n-1*>:0]	Stratix 10: <*n*> = 1, 2, 4, 8, 16 Arria 10, Stratix V:<*n*> = 1, 2, 4, 8
rx_in[<*n-1*>:0]	rx_in[<*n-1*>:0]	Stratix 10: <*n*> = 1, 2, 4, 8, 16 Arria 10, Stratix V:<*n*> = 1, 2, 4, 8

3.3 Read DMA Interface

Table 4. Read DMA Interface

Stratix 10	Arria 10, Stratix V	Comments
rd_dma_*	RdDMA*	Signal names differ, but functionality is the same unless otherwise noted below.
rd_dma_write_data_o[255:0]	RdDmaWriteData_o[<*n-1*>:0]	Stratix 10: Supports 256-bit interface only. Arria 10, Stratix V:<*n*> = 128 or 256
rd_dts_*	RdDTS*	Signal names differ for descriptor table slave interface, but functionality is the same unless otherwise noted below.

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Stratix 10	Arria 10, Stratix V	Comments
rd_dts_write_data_i[255:0]	RdDTSWriteData_i[<*n-1*>:0]	Stratix 10: Supports 256-bit interface only. Arria 10, Stratix V: <*n*> = 128 or 256
rd_dts_burst_count_i[4:0]	RdDTSBurstCount_i[<*n-1*>:0]	Stratix 10: Supports 256-bit bit interface only. Arria 10, Stratix V: <*n*> = 5 for a 256-bit interface. <*n*> = 6 for a 128-bit interface.
rd_dcm_*	RdDCM*	Signal names differ but functionality is the same.
rd_ast_rx*	RdAstRx*	Signal names differ but functionality is the same.
rd_ast_tx*	RdAstTx*	Signal names differ but functionality is the same.

3.4 Write DMA Interface

Table 5. Write DMA Interface

Stratix 10	Arria 10, Stratix V	Comments
wr_dma_*	WrDMA*	Signal names differ, but functionality is the same unless otherwise noted below.
wr_dma_read_data_o[255:0]	WrDmaReadData_o[<*n-1*>:0]	Stratix 10: Supports 256-bit interface only. Arria 10, Stratix V:<*n*> = 128 or 256
wr_dma_burst_count_i[4:0]	WrDMABurstCount_i[<*n-1*>:0]	Stratix 10: Supports 256-bit interface only. Arria 10, Stratix V: <*n*> = 5 for a 256-bit interface. <*n*> = 6 for a 128-bit interface.
wr_dts_*	WrDTS*	Signal names differ but functionality is the same unless otherwise noted below.
wr_dts_write_data_i[255:0]	WrDTSWriteData_i[<*n-1*>:0]	Stratix 10: Supports 256-bit interface only. Arria 10, Stratix V: <*n*> = 128 or 256
wr_dts_burst_count_i[4:0]	WrDTSBurstCount_i[<*n-1*>:0]	Stratix 10: Supports 256-bit interface only. Arria 10, Stratix V: <*n*> = 5 for a 256-bit interface. <*n*> = 6 for a 128-bit interface.

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Stratix 10	Arria 10, Stratix V	Comments
wr_dcm_*	WrDCM*	Signal names differ but functionality is the same.
wr_ast_rx*	WrAstRx*	Signal names differ but functionality is the same.
wr_ast_tx*	WrAstTx*	Signal names differ but functionality is the same.

3.5 Avalon-MM Slave Interfaces

Table 6. Avalon-MM Slave Interfaces

Stratix 10	Arria 10, Stratix V	Comments
txs_* hptxs_*	Txs	Stratix 10: includes 2 separate interfaces: • TXS: 32-bit non-bursting slave interface • HPTXS: 256-bit bursting slave interface Arria 10, Stratix V: includes a single TXS interface that can be 128-bit bursting, 64-bit bursting, or 32-bit non-bursting depending on the variant and settings.

3.6 Avalon-MM Master Interfaces

Table 7. Avalon-MM Master Interfaces

Stratix 10	Arria 10, Stratix V	Comments
rxm_bar_*	Rxm*	Signal names differ but functionality is the same unless otherwise noted below.
rxm_bar_<*m*>_writedata_o[<*n*>-*1*:0] rxm_bar_<*m*>_readdata_o[<*n*>-*1*:0]	RxmDataWrite_<*m*>_o[<*n*>-*1*:0] RxmReadData_<*m*>_o[<*n*>-*1*:0]	<*m*> is the BAR number, 0-5 <*n*> is the width of the bus Stratix 10: All BARs can be bursting, non-bursting, or disabled.<*n*> has the following values: • Non-bursting BAR: <*n*>=32 • Bursting BAR: <*n*>=256 Arria 10, Stratix V: Every BAR can be non-bursting or disabled. For non-bursting BARs <*n*> = 32. Only BAR2 supports bursting. If BAR2 is bursting <*n*>=128 for a 128-bit Avalon-MM interface. <*n*>=256 for a 256-bit Avalon-MM interface.
rxm_bar_<*m*>_byteenable_o[<*n*>-*1*:0]	RxmByteEnable_<*m*>_o[<*n*>-*1*:0]	<*m*> is the BAR number, 0-5. <*n*> is the width of the bus.

continued...

Stratix 10	Arria 10, Stratix V	Comments
		Stratix 10: All BARs can be bursting, non-bursting, or disabled. <*n*> has the following values: • Non-bursting BAR: <*n*>=4 • Bursting BAR: <*n*>=32 Arria 10, Stratix V: Every BAR can be non-bursting or disabled. For non-bursting BARs <*n*> = 4. BAR2 only supports bursting. If BAR2 is bursting <*n*>=16 for a 128-bit Avalon-MM interface. <*n*>=32 for a 256-bit Avalon-MM interface.

3.7 Control and Status Register Interface

Table 8. Control and Status Register Interface

Stratix 10	Arria 10, Stratix V	Comments
`cra_*`	`Cra*`	Signal names differ, but the functionality is the same unless otherwise noted below.
`cra_readdatavalid_o`	Not required	Stratix 10: `cra_readdatavalid_o` indicates that read data is valid. Arria 10, Stratix V: a read data valid signal is not necessary. Read data is guaranteed to be valid in the same clock cycle that the read is accepted by the slave interface.

3.8 Hard IP Reconfiguration Interface

Table 9. Hard IP Reconfiguration Interface

Stratix 10	Arria 10, Stratix V	Comments
`hip_reconfig_waitrequest`	Not required	Stratix 10: Signal names differ, but the functionality is the same unless otherwise noted below. Arria 10, Stratix V: A wait request signal is not necessary. Requests always complete in a deterministic number of clock cycles.
`hip_reconfig_readdatavalid`	Not required	Stratix 10: `hip_reconfig_readdatavalid` indicates that read data is valid. Arria 10, Stratix V: a read data valid signal is not necessary. Read data is guaranteed to be valid in the same clock cycle that the read is accepted by the slave interface.
`hip_reconfig_address[20:0]` `hip_reconfig_writedata[7:0]`	`hip_reconfig_address[9:0]` `hip_reconfig_writedata[15:0]`	Signal widths changed to correspond to the Stratix 10 transceiver implementation.

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Stratix 10	Arria 10, Stratix V	Comments
hip_reconfig_readdata[7:0]	hip_reconfig_readdata[15:0]	
Not required	ser_shift_load	Stratix 10: ser_shift_load is not required for dynamic reconfiguration on Stratix 10. Arria 10, Stratix V: You must toggle ser_shift_load once after changing to user mode before the first access to read-only registers. This signal should remain asserted for a minimum of 324 ns after switching to user mode.
Not required	interface_sel	Stratix 10: interface_sel is not required for dynamic reconfiguration on Stratix 10. Arria 10, Stratix V: interface_sel must be asserted when performing dynamic reconfiguration. Drive interface_sel low for 4 clock cycles after the release of ser_shift_load.

3.9 Interrupt Interface

Table 10. Interrupt Interface

Stratix 10	Arria 10, Stratix V	Comments
Not available	app_int_ack	Stratix 10: No ACK generated for legacy interrupts. User logic must form and parse packets.
int_status[7:0]	int_status[3:0]	Stratix 10: Supports legacy interrupts A, B, C, and D. Supports the following 4 additional status signals: • [4]: RC AER error interrupt status • [5]: Root complex PME interrupt status • [6]: Asserted when hot plug event occurs and PME is enabled • [7]: Hot plug event interrupt status Arria 10, Stratix V: Supports Legacy Interrupts A, B, C, and D.
int_status_common[2:0]	Not supported	Stratix 10: Supports the following 4 status indicators: • [0]: Interrupt status for autonomous bandwidth status register • [1]: Interrupt status for bandwidth management status register • [2]: Interrupt status for link equalization request bit in the link status register

3.10 Error Interface

Table 11. Error Interface

Stratix 10	Arria 10, Stratix V	Comments
tx_par_err	tx_par_err[1:0]	Stratix 10: The TX Transaction Layer or TX Data Link Layer asserts tx_par_err to indicate a parity error. Arria 10, Stratix V: The following encodings are defined: • 2'b10: TX Transaction Layer detects a parity error 2'b01: TX Data Link Layer detects a parity error
derr_uncor_ext_rcv	Not supported	Stratix 10: When asserted, indicates an uncorrectable 2-bit ECC error in the RX buffer. Arria 10, Stratix V: Not supported.
Not supported	cfg_par_err	Stratix 10: Not supported. Arria 10, Stratix V: Indicates a parity error in a TLP routed to the internal Configuration Space. This error is also logged in the Vendor Specific Extended Capability Internal Error register. You must reset the IP core if this error occurs.

3.11 Status and Link Training Interface

Table 12. Status and Link Training Interface

Stratix 10	Arria 10, Stratix V	Comments
ltssmstate[5:0]	ltssmstate[4:0]	Stratix 10: Provides finer granularity and different encoding. For example, L0 is now 0x11 instead of 0x0F. Refer to user guide for complete mapping.
link_up	Not supported	Stratix 10: Adds bit for x16 configuration.
Not supported	ev128ns ev1us hotrst_exit l2_exit dl_up	Stratix 10: Not supported Arria 10, Stratix V: Refer to the Arria 10 PCIe user guides for more information.

Related Links

- Stratix 10 Avalon-ST Interface for PCIe Solutions User Guide
- Stratix 10 Avalon-MM Interface for PCIe Solutions User Guide

3.12 PHY Interface for PCI Express (PIPE) Interface

Table 13. PIPE Interface

Stratix 10	Arria 10, Stratix V	Comments

`rxeqeval`
`rxeqinprogress`
`invalidreq`
`dirfeedback[5:0]` (H-Tile only)
`sim_pipe_mask_tx_pll_lock`
	Not supported	Stratix 10: The PIPE interface is compliant to the *PHY Interface for the PCI Express Architecture PCI Express 3.0*.

`sim_ltssmstate[5:0]`	`sim_ltssmstate[4:0]`	Stratix 10: Provides finer granularity and different encodings. For example, L0 is now 0x11 instead of 0x0F.
Not required	`eidleinfersel0[2:0]`	Stratix 10: Not required. The PIPE interface is compliant to the Gen3 PIPE specification. Arria 10, Stratix V: Indicates Electrical Idle entry inference mechanism selection.

3.13 Test Interface

Table 14. Test Interface

Stratix 10	Arria 10, Stratix V	Comments

`test_in[66:0]`
`aux_test_out[6:0]`
`test_out[255:0]`
	`test_in[63:0]`	Stratix 10:
		• `test_out[255:0]`: available only in x16 configuration
		• `aux_test_out[6:0]`: available in x8 or smaller configurations

Document Revision History

Date	Version	Changes
January 2017	17.0 IR2	• Initial release