Mobile SDRAM Interface Using MAX II CPLDs

Introduction

This application note details the implementation of a mobile SDRAM interface using an Altera® MAX® II CPLD.

Mobile SDRAM

SDRAM provides high-density storage at low cost. Mobile SDRAM devices are different in that they also have low-power utilization. This is made possible by the additional power saving features offered by SDRAMs, for example:

- Temperature compensated self refresh (TCSR)
- Partial array self refresh (PASR)
- Deep power-down mode

SDRAM's are used in a wide range of portable electronic devices such as digital cameras, mobile phones, medical equipment, home electronics, and other devices. This application note describes a generic interface between a microprocessor and a mobile SDRAM device. You can easily integrate it into applications to equip them with the advantages of SDRAMs.

SDRAM Interface

This design enables a MAX II CPLD to function as an interface between a microprocessor and a mobile SDRAM. The microprocessor commands are interpreted appropriately, and the appropriate signals, per the timing requirements, are interfaced to the SDRAM in a format that it recognizes. Figure 1 illustrates the basic arrangement for this interface. Interface signals on the memory are for a typical Micron SDRAM device.

Figure 1. Mobile SDRAM Interface
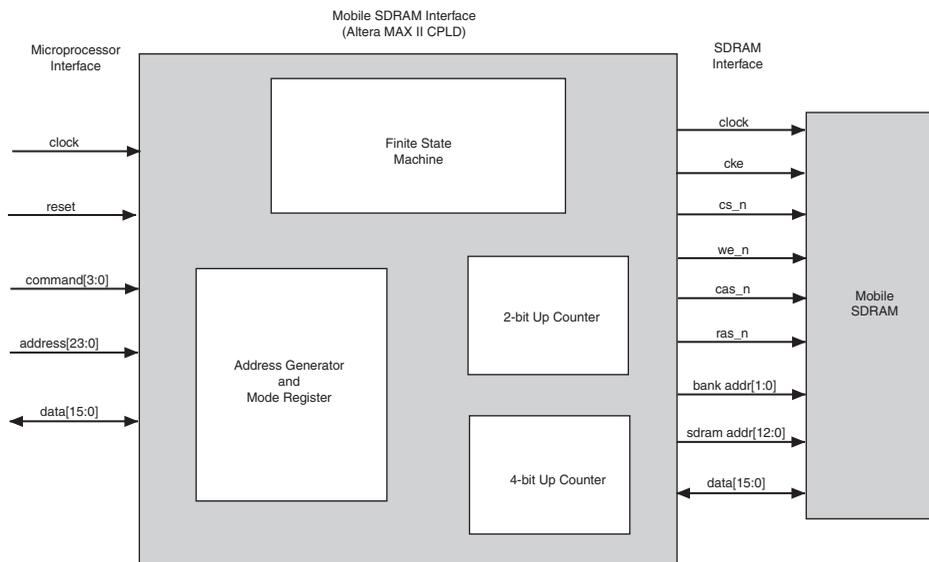
The various signals comprising the microprocessor and SDRAM interfaces are described in Table 1.

Table 1. Mobile SDRAM Signals (Part 1 of 2)			
Pin	**Size**	**Type**	**Description**
`clk`	1 bit	Input	System clock.
`cke`	1 bit	Input	Clock enable. Activates and de-activates the clock.
`cs_n`	1 bit	Input	Chip select. Enables or disables the command decoder.
`we_n, cas_n, ras_n`	1 bit	Input	Command pins. They select the mode of operation.
`bank_address`	2 bits	Input	Defines the bank to be accessed.
`sdram_address`	13 bits	Input	Row and column addresses are asserted depending on whether the active or read and write commands are asserted.
`data`	16 bits	Input/Output	Data input and data output.

Table 1. Mobile SDRAM Signals (Part 2 of 2)			
Pin	**Size**	**Type**	**Description**
clock	1 bit	Input	The same clock that drives the processor also drives the controller.
reset	1 bit	Input	External active high input to reset the controller.
command	4 bits	Input	These four lines give commands to the controller. Details of the commands are available in the Mobile SDRAM data sheets from Mircon.
address	24 bits	Input	The most significant 2 bits indicate the bank, the next 9 bits indicate the row address, and the remaining 13 bits indicate the column address.
data	16 bits	Input/Output	Bi-directional data bus of 16-bits width.

The mobile SDRAM interface design consists of four main modules, as shown in Figure 1. These are the finite state machine (FSM) module, a 2-bit up counter, a 4-bit up counter, and the address generator and mode register. These modules are briefly described in the following sections.

Finite State Machine

The finite state machine interprets the inputs from the microprocessor and sends the appropriate command to the mobile SDRAM device along with the address per the timing requirements. The mobile SDRAM device then goes to the appropriate state and executes the command.

2-Bit Up Counter

This counter monitors the number of clock cycles for CAS latency. The latency can be up to two clock cycles.

4-Bit Up Counter

This counter monitors the number of clock cycles during the read and write burst operation. The burst lengths can be one, two, four, or eight.

Address Generator and Mode Register

The address generator maps the address provided by the microprocessor to the mobile SDRAM device in the required format. It generates the bank, row, and column address separately, depending on the state, and passes it on to the mobile SDRAM device.

The mode register and extended mode register contents are shown in Tables 2 and 3.

Table 2. Mode Register Contents			
Pin	**Size**	**Type**	**Description**
`burst_length`	2 bits	Input	Provides the option to choose between burst lengths of 1, 2, 4, or 8 locations.
`burst_type`	1 bit	Input	Provides the option to select between sequential access and interleaved access.
`CAS_latency`	2 bits	Input	Provides the option to allow delays of 2 or 3 clock cycles after sending the read command.

Table 3. Extended Mode Register Contents (Part 1 of 2)			
Pin	**Size**	**Type**	**Description**
PASR	3 bits	Input	Partial array self-refresh. Provides options to refresh the four banks, two banks, single bank, half bank, and quarter bank. Details of the commands are available in the Mobile SDRAM data sheets for Micron.

Table 3. Extended Mode Register Contents   (Part 2 of 2)

Pin	Size	Type	Description
TCSR	2 bits	Input	Temperature compensated self-refresh. Allows the controller to program the refresh interval, depending on the temperature of the BATRAM device. Details of the commands are available in the Mobile SDRAM data sheets from Micron.
driver_strength	1 bit	Input	Used for output driver strength selection. Full-drive strength can drive loads of up to 50 pF. Half-drive strength is suitable for point-to-point applications. ● 0 = half strength ● 1 = full strength

Implementation

This design can be implemented using the MAX II EPM570 device (with 144 pins or more). The design source code is compiled and can be programmed into the MAX II CPLD. Host interfacing ports and SDRAM interfacing ports are shown in Figure 1. This SDRAM interface design utilizes approximately 24% of the logic elements (LEs) in an EPM570 device and uses up to 85 I/O pins.

Source Code

This design has been implemented in Verilog HDL. The source code, test bench, and complete Quartus® II project are available at:

www.altera.com/literature/an/an499_design_example.zip

Conclusion

As illustrated throughout this design, MAX II CPLDs are a great choice for implementing interfaces to memory devices such as the Mobile SDRAM. Their low cost, easy power-on, multi-volt features, and most significantly, their low power requirements, make them the ideal programmable logic devices to implement such memory device interfacing applications.

Additional Resources

The following are additional resources for this application note:

■ MAX II CPLD home page:
http://www.altera.com/products/devices/cpld/max2/mx2-index.jsp

■ MAX II Device Literature page:
http://www.altera.-com/literature/lit-max2.jsp

■ MAX II Power-Down Designs:
http://www.altera.com/support/examples/max/exm-power-down.html

■ MAX II Application Notes:
AN 428: MAX II CPLD Design Guidelines
AN 422: Power Management in Portable Systems Using MAX II CPLDs

Document Revision History

Table 4 shows the revision history for this application note.

Table 4. Document Revision History		
Date and Document Version	**Changes Made**	**Summary of Changes**
December 2007, v1.0	Initial release.	—