

LED Blink Using Power Sequencing in Altera MAX Series

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Altera® MAX® II, MAX V, and MAX 10 devices can be used in this example application.

Powering components off and on—with minimal system intervention, also known as blink—is a valuable power savings technique. The supported Altera devices are well suited for this due to their simple power sequencing and proprietary features. This application note illustrates a simple method for blinking an LED by using the auto stop and auto start capability of the supported Altera devices.

Related Information

- [Design Example for MAX II](#)
Provides the MAX II design files for this application note (AN 498).
- [Design Example for MAX 10](#)
Provides the MAX 10 design files for this application note (AN 498).
- [Power Management in Portable Systems Using MAX II CPLDs](#)
- [MAX II CPLD Design Guidelines](#)

Power Saving Using Auto Stop and Auto Start

Many consumer and industrial application systems do not require the device to be powered on at all times. In fact, it is preferable to have a system in which the device powers on intermittently, as and when required only, and remains off for most of the cycle. The supported Altera devices are designed to tolerate any possible power-on sequence. They also have one of the industry's lowest power-up timing characteristics (typically 200 microseconds for the EPM240 device, depending on the density of logic in the design). The MAX 10 Single Supply devices are designed for you to easily manage the power-up sequence on the board. The MAX 10 Single Supply devices support instant-on feature, which is the fastest power-up mode for MAX 10 devices.

This makes the supported Altera devices the perfect target device for such a system. The device can be turned off when a task is complete and switched back on again for its next task. The self power down is caused by the device itself, while the auto power up is caused by an external circuitry such as a simple RC circuit designed for the required delay. The entire scheme finds context in power savings, typically in battery operated systems which may be used for functions that are cyclical or periodic in nature (such as sampling for parameters in a telemetering system), where the power can be turned off when the device can afford to take a break.

The device generates two signals, power down and its complement to cause self power down by triggering an external circuit to shutdown the LDO supplying power to the device. After the device is off, the

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external circuit powers it back on after the designed delay of the external RC circuit. An LED glows upon power on and switches off after the device is powered down.

Figure 1: Implementing a Power-Down Circuit with the Supported Altera Devices

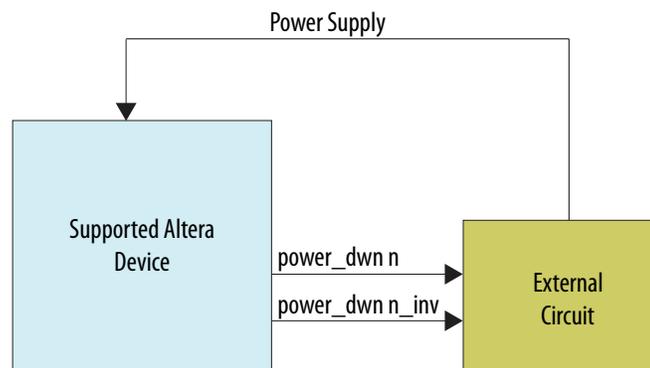
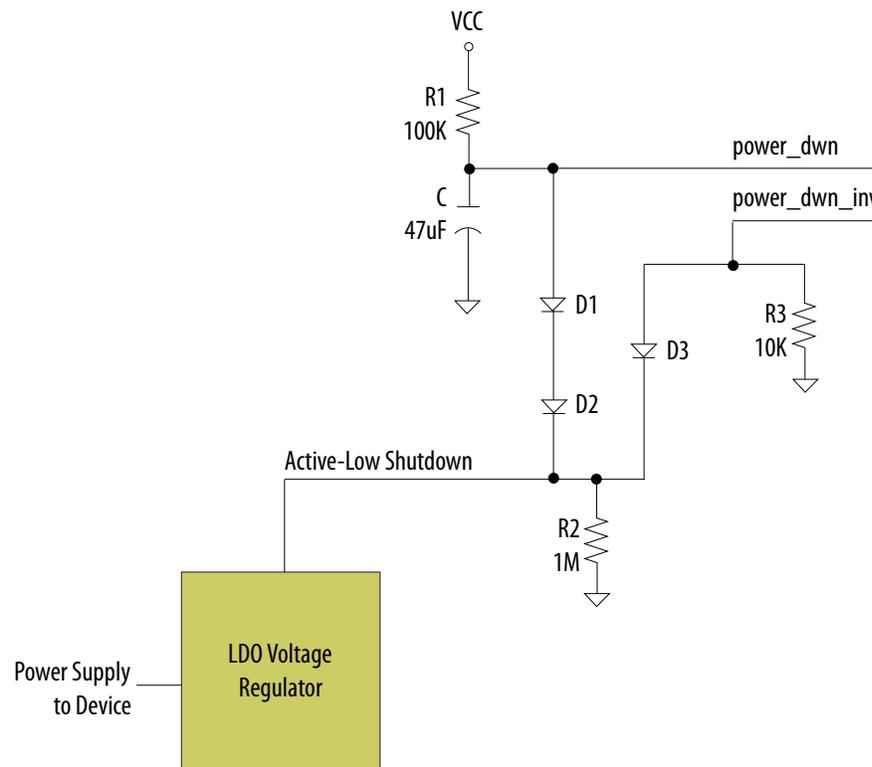


Figure 2: External Circuitry for a Power-Down Circuit with the Supported Altera Devices



This section describes the self-power-down and auto-power-up capability of the supported Altera device. An LED indicates power to the supported Altera device. When the device is on, the `power_down` signal is low (`power_down_inv` is high). The shutdown pin on the LDO is inactive (active low) and the LDO continues to remain on. Capacitor C is kept in its discharged condition.

To switch off the device, the `power_dwn` signal goes high (`power_dwn_inv` goes low). This causes the LDO to shutdown, and thereby switching off the device. The I/O pins on the device get tri-stated, releasing the pull down on the capacitor. The capacitor starts charging with the time constant $R1 \cdot C$. It charges until the voltage across it remains less than the threshold potential of the shutdown pin on the LDO (enhanced by voltage drops across diodes D1 and D2). When the threshold is reached, the LDO turns on and, consequently, the supported Altera device turns on. This cycle continues to repeat itself.

Implementation

The detail description of the implementation is based on the MAX II devices. This application can also be implemented in MAX V and MAX 10 devices.

You can implement the steps in this application note with an EPM240G device, or any other MAX II device, simple external RC circuitry, and a power supply regulator that has shut-down capability. Implementation involves using this example's source code and allocating the appropriate signal and control lines to the general purpose I/O (GPIO) lines of the MAX II device along with its support circuitry. The demo board MDN-B2 is a board with such support circuitry built-in. An LED on the demo board is made to indicate the power status of the MAX II device. The demo board also facilitates power measurements by allowing measurement of voltage drops across a 1- Ω resistor in series with the MAX II device core power supply.

Table 1: MAX II Example Implementation

EPM240G Pin Assignments	
Signal	Pin
<code>power_on_led</code>	69
<code>power_down_inv</code>	12
<code>power_down</code>	14

Unused pins are assigned as **input tri-stated** in the Quartus II software's device and pin option settings prior to compilation.

Design Notes

To demonstrate this design on the MDN-B2 demo board, follow these steps:

1. Turn on the power to the demo board (using the slide switch SW1).
2. Download the design to the MAX II device through the JTAG header JP5 on the demo board and a conventional programming cable (ByteBlaster™ II or USB-Blaster™). Keep SW4 on the demo board pressed before and during the start of the programming process. Once complete, turn off the power and remove the JTAG connector.
3. Switch on power to the demo board (using the slide switch SW1) and observe VCCINT and VCCIOs being cyclically powered down and powered up.
4. Observe the LEDs D2 glow each time the power to device is restored.
5. Measure the voltage drops across R52 for the 2.5 V power supply (pads TP1 and TP2) and across R27 for the 1.8 V power supply (pads TP3 and TP4).

Acknowledgments

Design example adapted for Altera MAX 10 FPGAs by:

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Document Revision History

Date	Version	Changes
September 2014	2014.09.22	Added MAX V and MAX 10 devices.
December 2007	1.0	Initial release.