Power Sequence Auto Start Using Altera MAX Series

2014.09.22

AN-491 Subscribe Send Feedback

This design example describes a simple method for implementing Auto Start using Altera® MAX® II, MAX V, and MAX 10 devices.

The supported Altera devices are an excellent choice for implementing low power applications and when battery life extension are of importance. These devices are well suited for this technique because of their simple power sequencing and proprietary features.

Related Information

- **Design Example for MAX II**
  Provides the MAX II design files for this application note (AN 491).
- **Design Example for MAX 10**
  Provides the MAX 10 design file for this application note (AN 491).
- **Power Management in Portable Systems Using MAX II CPLDs**
- **MAX II CPLD Design Guidelines**

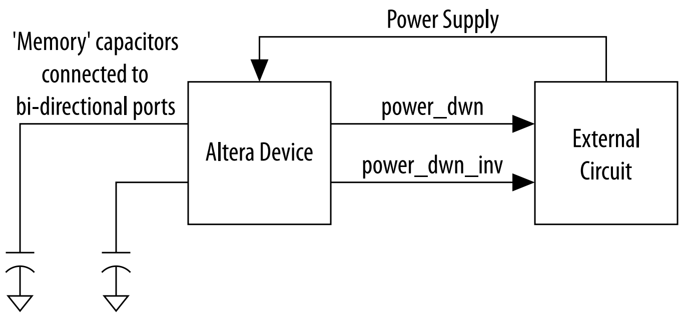
Power Saving

Many consumer and industrial application systems do not require the device to be powered on at all times. It is preferred to have a design in which the device powers on intermittently, remaining off for most of the cycle. This is especially useful in portable battery-operated systems which can function on a non-continuous periodic task.

Because MAX II and MAX V devices do not require a special power-on sequence, they can be switched on quickly (typically 200 µs, depending on the logic density). The ability to switch on and off quickly allows you to completely switch off the device and switch it back on using external circuitry. The external circuitry can be a simple RC timer designed for the required delay. The MAX 10 Single Supply devices are designed for customer to easily manage power-up sequence on the board. The instant-on feature is the fastest power-up mode for MAX 10 devices.

However, if you implement considerable power off time, such a simple RC timer circuit is not practical. This requires very large values of R & C. A counter utilizing capacitors as memory elements extends the power-down period. The device turns on for a very small duration during this power-down period, reads the value in these capacitors, increments the count, and stores them back again before powering down. This cycle repeats itself until the desired count is reached, at which time the device switches on completely. When it switches on in the power-on period, the device executes the task it was designed to accomplish.

Figure 1: Basic Block Diagram of an Auto Start System

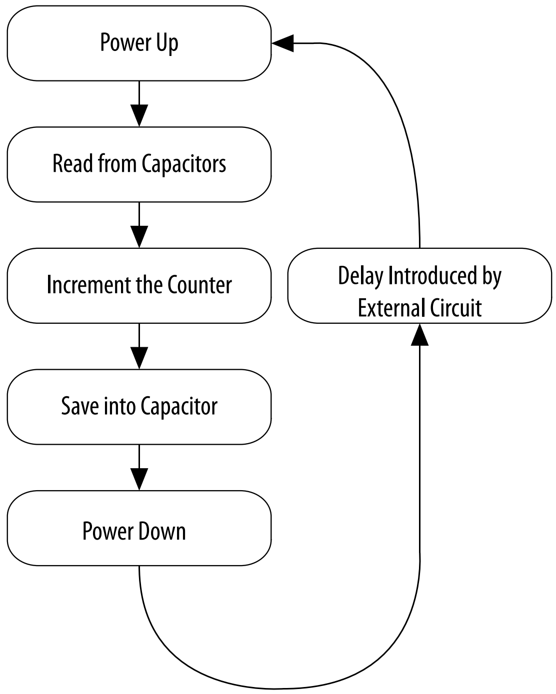


The device uses the power down signals (`power_dwn` and its complement) to trigger the external circuit and power down the device. After the designed delay, the external circuit powers on the device. The memory capacitors are connected to the bidirectional pins of the device and are used as non-volatile memory elements.

Auto Start

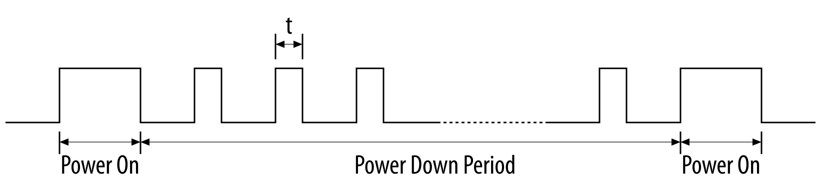
As soon as the device is powered on, it goes into the read state. The value on the capacitors is read and stored in registers. This implementation uses two capacitors that allow you to store four different values. One of the four LEDs used is switched on after the read operation that corresponds to the value read from the capacitors. This value or count is incremented and stored back into the capacitors, which act as non-volatile memory elements. Power down is then initiated by setting the `power_dwn` pin high. When power down is complete, the external RC circuit acts as a timer and activates the device. This is repeated until the desired delay is obtained (desired count is reached) and the complete effective stretching of the power-down time is achieved (four times in this case). The duty cycle of operation of the device can be controlled, resulting in a longer power-down period and thereby decreasing the overall power consumption.

Figure 2: Auto Start Operation Flowchart



Power Cycle

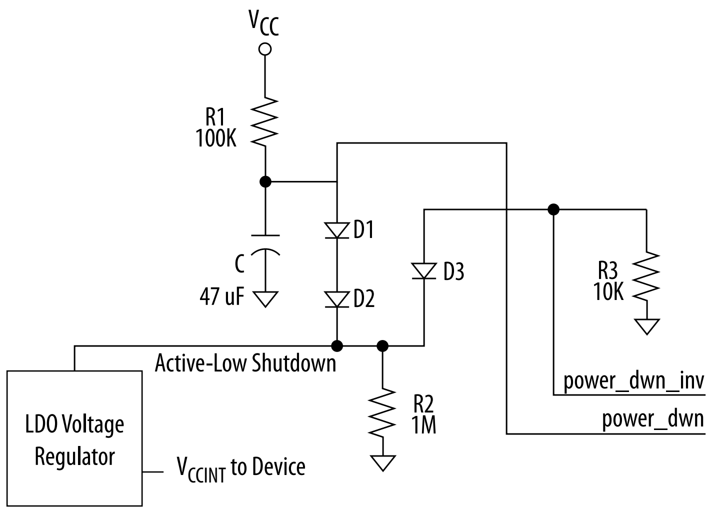
Figure 3: Power Cycle Waveform



Each cycle consists of a 'Power On' and a 'Power Down' period. In the 'Power Down' period the MAX II devices regularly switches on for a very small period of time 't', increments the counter, and switches off. When the desired count is reached, the MAX II devices enter into the Power On period and reinitializes the value of the counter. It then performs the desired functions. At the end of the 'Power On' period, the capacitors contain the reinitialized value. When the MAX II devices are powered on again, it increments the counter and shuts down after the period 't', and the count is restarted.

External Circuits

Figure 4: External Circuitry



When the `power_dwn` signal is low (`pwr_dwn_inv` is high), the voltage regulator (which has an active low shutdown control) is switched on and the capacitor C discharges. Whenever the device wants to switch off, it makes the `power_dwn` signal high (`pwr_dwn_inv` is low). This switches off the voltage regulator, cutting off the power to the device.

When all the I/O pins of the device are tri-stated, the capacitor starts charging. It charges until the voltage across the device remains less than the threshold potential of the regulator's shutdown control (enhanced by diodes D1 and D2), When the threshold is exceeded, the voltage regulator is switched on. The cycle repeats itself.

Auto Start Using MAX II Devices

The detailed description of the implementation is based on the MAX II devices. This application can also be implemented in MAX V and MAX 10 devices.

You can implement this design example with an EPM240 or any other device, supporting external RC circuitry, a power supply that is capable of shut down, and two capacitors on the GPIO pins to act as 'memory' devices that save previous states. Implementation involves using the design example source code and allocating the appropriate signals and control lines to the GPIO lines of the MAX II device, along with its support circuitry. The MDN-B2 demo board has a built-in support circuitry.

To demonstrate the control of the power cycle, two capacitors (C9 and C10 on the MDN-B2 demo board) and four LEDs (D2, D3, D5, and D6) are used. This design reads the values from the capacitors as soon as the MAX II is powered on.

Table 1: LED Mapping

Capacitor C9	Capacitor C10	LED
0	0	D2

Capacitor C9	Capacitor C10	LED
0	1	D3
1	0	D5
1	1	D6

For each set of values, the corresponding LED glows. The MAX II then increments the count and writes back this value to the capacitors. The write cycle continues for some time to ensure sufficient charging of the capacitors. The power down and its complement signals are made high and low, respectively, resulting in complete power down.

Upon subsequent power on after a period of time determined by the external RC, the MAX II repeats the cycle of reading, LED display, and updating the capacitor states before powering down again. Observing the LED counting up demonstrates the Auto Start feature of this design.

Table 2: EPM240G Pin Assignments

Assign unused pins **As input tri-stated** in the **Device and Pin Options** dialog box in the Quartus II software prior to compilation.

Signal	Pin
`cap_a`	Pin 83
`led1`	Pin 69
`led3`	Pin 71
`pwr_dwn`	Pin 14
`cap_b`	Pin 84
`led2`	Pin 70
`led4`	Pin 72
`pwr_dwn_inv`	Pin 12

Auto Start Design Demonstration on MDN-B2 Board

To demonstrate the design example on the MDN-B2 demo board, follow these steps:

1. Ensure that V_{CCIO} voltages on both banks are set to 2.5V (jumpers on JP9 and JP7 on the demo board are set to 2.5V).
2. Turn on the power to the demo board (using slide switch SW1) and download the design on to the MAX II device through the JP5 JTAG header and a conventional programming cable such as the ByteBaster™ II or USB-Blaster™.
3. Keep SW4 on the board pressed as you begin the programming process.
4. Turn off power to the board and remove the JTAG connector after programming.
5. Turn on the power to the demo board. Using a voltmeter between TP3 and GND on the demo board, observe V_{CCINT} being powered down and powered up cyclically.
6. Repeat observation for V_{CCIO} (between TP1 and GND on demo board). Also observe the 4 LEDs (D2, D3, D5, and D6) shift their position each time the power to the device is restored.
7. Each time the LED blinks, its position is based upon the previous LED position that blinked and in accordance to the LED Mapping table.

Acknowledgments

Design example adapted for Altera MAX 10 FPGAs by:

Orchid Technologies Engineering and Consulting, Inc.

Maynard, Massachusetts 01754

TEL: 978-461-2000

WEB: **www.orchid-tech.com**

EMAIL: **info@orchid-tech.com**

Document Revision History

Date	Version	Changes
September 2014	2014.09.22	• Added MAX V and MAX 10 devices. • Updated template. • Restructured document.
December 2007	1.0	Initial release.