

Solution Brief

Avionics and Defense
Computing for Unmanned Aerial Vehicles



Delivering Certified, Safety-Critical Computing for the Future of Aviation

DDC-I's Deos RTOS for Avionics leverages 11th Gen Intel® Core™ processors to drive a new generation of safety-critical UAV computing technology, certifiable to fly in metropolitan and commercial airspaces.



"The Intel® Core™ i7 processor's high-performance multicore architecture, on-chip graphics, and AI processing, together with the availability of certification data, are very attractive to our avionics customers. Our SafeMC multicore technology leverages many of these capabilities, employing techniques such as cache partitioning, memory pools, time-space partitioning, and slack scheduling. Together these capabilities provide an efficient, robust, and deterministic platform that builds on Intel® technology to maximize performance while delivering a certifiable multicore environment that reduces multicore interference and worst-case responses."

—Greg Rose, vice president of marketing and product management at DDC-I

Imagine a world where packages are delivered by unmanned aerial drones, ride services are provided by autonomous air taxis, and the latest mission-critical technology is a rugged autonomous aircraft. These types of futuristic aircraft require more than flight controls. They must also maneuver with the utmost safety.

Accordingly, unmanned aerial vehicles (UAVs) are equipped with high-end sensors to enable airspace visibility, identify and track other objects, and reroute when needed. With autonomous vehicle innovations fast emerging, safety-critical technologies are in high demand both commercially and for defense applications, and the market for them is growing rapidly as a result.

Consider the technological and regulatory requirements governing the market for electric vertical takeoff and landing (eVTOL) UAVs. Flight safety is the avionics industry's highest priority, and DO-178C/254 certifications are required to demonstrate the design assurance of all electronic hardware in airborne systems. Small yet high-compute sensors for detect-and-avoid applications are essential to safe air taxi operation. Ultimately, these types of aircraft must be DO-178C/254 certifiable to fly in metropolitan areas and commercial airspaces.

Challenges: Meeting the industry's certification standards with high-speed multicore processors

The avionics industry is transitioning from single-core processors to multicore processors for safety-critical electronic systems. The performance limitations of single-core processors hinder the ability of applications and systems to consolidate, which is required to minimize size, weight, power, and cost (SWaP-C). By design, multicore processors offer increased computing power without significant increases in SWaP-C, which makes them better suited for aviation-embedded applications.

However, safety-critical electronic systems using multicore processors can be more challenging to certify because of their complexity. Multicore processor interference paths rise exponentially as core counts rise due to interactions between applications and other platform resources such as system memory and I/O.

When this is the case, nondeterministic behavior can occur for the applications running on the cores. Safety-critical processing requires programs to be executed deterministically. Ultimately, the amount of computing taking place in each execution period should be verifiable and guaranteed through a process known as time (or temporal) partitioning.

Currently, only a few multicore platforms have been certified to the highest design assurance level (DO-178C DAL A or DAL B), which is required for flight-critical operations. All cores on these platforms are active and capable of running safety-critical applications. However, exact guidance from the certifying authorities (FAA, EASA, and TC) is not prescriptive and has yet to be tested through the flight certification process.

Consider also the limited number of commercial off-the-shelf (COTS) multicore processors that are specifically designed for safety-critical avionics. Ultimately, it's the responsibility of system integrators to ensure the performance of multicore processors in safety-critical environments.

The solution: DDC-I's Deos time and space partitioned real-time operating system

To enable safety-critical avionics applications, DDC-I offers the Deos time and space partitioned real-time operating system (RTOS), which has been verified for compliance with DO-178C/ED-12C Design Assurance Level A (DAL A) for avionics applications. Deos RTOS supports ARINC 653 APEX and rate monotonic scheduling (RMS) and is targeted for the Future Airborne Capability Environment (FACE) safety base profile.

Since its initial verification and audit to DAL A by Transport Canada in 1998, Deos has been tested and field proven as a safety-critical RTOS. Today, Deos RTOS is certified and flying in tens of thousands of aircraft. The technology has advanced significantly over time while continuing to pass the required audits of the world's governing certification authorities, including the FAA, ENAC, JAA, EASA, CAAC, and the Airframe and Avionics Supplier Designated Engineering Representatives (DERs).¹

DDC-I's newest Deos RTOS version enables multiple core use on a microprocessor for time and space partitioned safety-critical applications. This is achieved in part by bounding the cross-core contention between cores that is caused by shared resource interference patterns and tight scheduling control. The bounding process allows users to identify and minimize shared resource interference.

Bounding and controlling execution with Deos SafeMC technology

Analysis has proven that the cache effects from resource sharing contribute significantly to unbounded cross-core contention. To address this issue, DDC-I has developed SafeMC technology, which manages, bounds, and controls execution on multicore processors to enable safety-critical processing.

SafeMC uses its patented memory pooling and cache partitioning to tightly control cache usage. It also partitions the caches for the applications, providing the resource and scheduling mechanisms to enable developers to bound and control the interference patterns that occur whenever processor cores share resources such as cache, memory, and I/O.

As a result, developers can isolate cache at the application/partition level using software configuration files. Because of this patented technology, Deos developers have full use of all cores for safety-critical operation, with no need to designate specific cores to particular DAL assurance levels. Cache partitioning doesn't require specific processor hardware or configuration settings and can work with technologies such as Intel® Cache Allocation Technology (CAT).

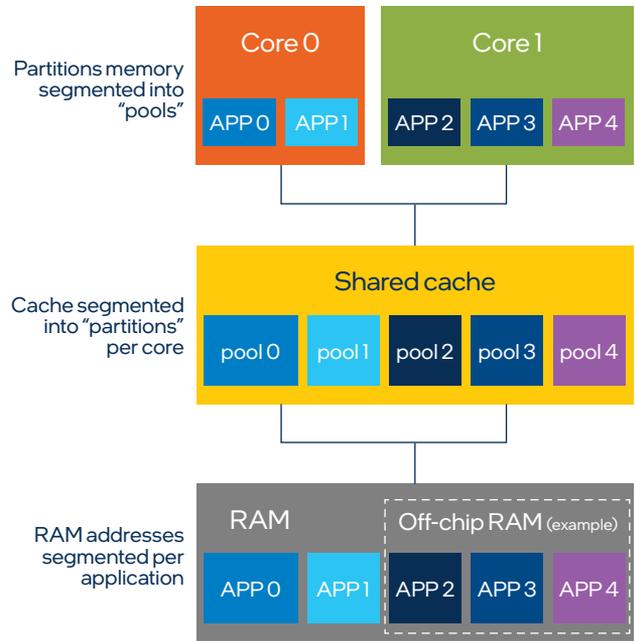


Figure 1: SafeMC memory pools and cache partitioning.

Bounding cross-core contention with Safe Scheduling

To mitigate the challenges related to safety-critical applications, Deos employs bound multiprocessing as well as Safe Scheduling. Bound multiprocessing enables scheduling control of an asymmetric multiprocessing model while preserving the hardware abstraction and managing symmetric multiprocessing. This allows the user to specify which processors a thread can run on. With tight control over execution, application developers can design a system that bounds and minimizes worst-case execution, which, in turn, enables multicore processors to support safety-critical processing.

Safe Scheduling works as follows: Its two-level scheduling model employs one scheduler per core, with all schedulers synchronized across the cores. Scheduling tasks on individual cores bound, or even eliminate, cross-core contention. At the first level, time is managed in windows, which are aligned across all cores. Within a time window, second-level schedulers such as ARINC 653, Deos RMA, and POSIX are assigned to each core. Applications are then assigned to one or more of the schedulers.

Each scheduler can run multiple tasks in multiple processes/partitions. As a result, developers can orchestrate the scheduling of applications running on different cores and different windows with limited interference. Safe Scheduling offers a configurable approach by having a single RTOS instance manage all cores. It also allows users to control how tasks are coscheduled across the cores.

As shown in Figure 2, this scheduling environment enables DAL applications to run simultaneously across all cores by allowing the system integrator to configure systems that minimize and bound resource contentions between processor cores. For the avionics industry, this functionality allows developers to efficiently use multicore processors while also expediting the certification process.

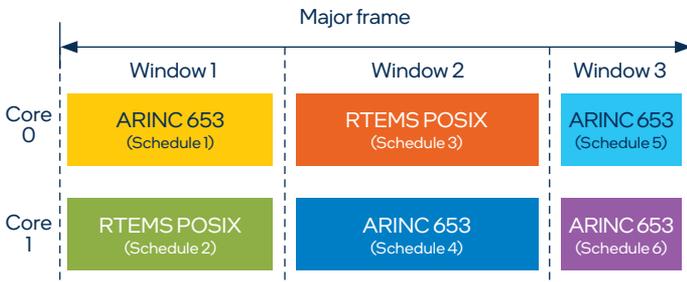


Figure 2: DDC-I Deos Safe Scheduling.

Leveraging 11th Generation Intel® Core™ system-on-a-chip (SoC) technology

Deos certifiable RTOS supports 11th Gen Intel® Core™ SoC technology with an integrated graphics processing unit (GPU). 11th Gen Intel® Core™ processors deliver high performance CPU/GPU computing with integrated AI acceleration. They also support high-speed processing for low-latency deterministic computing. 11th Gen Intel Core processors provide the right balance between performance and responsiveness in a reduced-power platform. 11th Gen Intel Core SoCs redefine Intel® CPU performance with high-speed wireless and wired connectivity and advanced tuning features.

Ultimately, 11th Gen Intel Core processors provide the scalable multicore processing required to certify safety-critical applications to DO-178C Design Assurance Level (DAL) A. These SoCs provide an integrated GPU for a significant performance and SWaP advantage over legacy CPUs lacking on-chip GPUs.

With 11th Gen Intel Core processing technology, Deos RTOS allows developers to create new, advanced displays and sensors that would otherwise be more difficult to design and certify for safety-critical operation. And with the processor's large cache, the Deos cache partitioning becomes a powerful tool to optimize the performance of real-time applications, without imposing on hardware configuration settings.

Key Deos and 11th Gen Intel Core processor features:

- DO-178 and DO-254 certification packages
- High compute performance with low power consumption
- SoC with integrated GPU
- Minimized size, weight, and power (SWaP)

Avionics industry standards and other modules:

- DO-178C/ED-12C Verification Evidence to Design Assurance Level A (DAL A)
- ARINC 653 (ARINC Specification 653 Part 1)
- Conformant to FACE 3.1 Technical Specification for the Operating System Segment (OSS)
- POSIX 1003.1 subset targeted at FACE Security, Safety Base, and Safety Extended Profiles
- File System (ARINC Specification 653 Part 2)
- Certifiable Fast File System (CFFS) – High Throughput Data Streaming File System
- Deos Volume Management System (DVMS) – High Performance Random Access File System

Intel and DDC-I: A partnership to drive innovation

DDC-I has engineered Deos for Intel® IA-32 processors since its first DO-178C DAL A certification baseline in 1998, which was developed for the Intel® Pentium® platform and used on the Bombardier Global Express. Since then, DDC-I has supported multiple Intel® processors, including Intel Pentium, Intel Atom®, Intel® Xeon® processors, and now high-performance 11th Gen Intel Core processors. For years, avionics customers have relied on the Deos solution, and today it drives safety-critical applications that deliver all the performance of Intel's most advanced processors.

With Intel® Core™ i7 processors, Deos extends its existing support for Intel Atom and Intel Xeon processors through to 11th Gen Intel Core processors. Deos provides a common certification package and development tools across all Intel processors, including support for DDC-I's DO-330-qualified tools.

The 11th Gen Intel Core i7 SoC processor combines four cores operating at up to 4.4 GHz with an integrated Intel® Iris® X^e graphics processor and up to 12 MB of cache. AI/DL instruction sets are included as well, with Vector Neural Network Instructions (VNNI) and support for the Intel® Distribution of OpenVINO™ toolkit. Intel Core i7 processors also provide four PCIe 4.0 lanes and support DDR4 and LPDDR4x with optional in-band error correction code (ECC). Other benefits of 11th Gen Intel Core processors include:

Increased performance across the board: Built on Intel® third-generation, 10 nm microarchitecture, 11th Gen Intel Core processors post up to a 23 percent gain in single-thread performance, up to a 19 percent gain in multithread performance, and up to 2.95x the graphics performance vs. 8th Gen Intel® Core™ processors.²

Multiple real-time workloads with minimal jitter: The combination of the 11th Gen Intel Core processor and Intel Iris X^e graphics performance is complemented with hardware-based acceleration to simultaneously handle multiple compute-heavy tasks. This orchestrated system maximizes hardware resources efficiently for near-real-time, multiworkload performance with minimal jitter.

Accelerated AI inferencing: 11th Gen Intel Core processors deliver accelerated AI inferencing in parallel with other core functions. AI and deep learning inferencing can run on up to 96 graphic execution units on the CPU with VNNI, which condenses three Advanced Vector Extensions (AVX) instructions into one.

Built-in hardware-based security: Intel provides security at the platform boot level, security for data at rest on the platform, and security for data in flight. New security features such as Intel® Total Memory Encryption (Intel® TME) complement the capabilities of Intel® Boot Guard.

Conclusion: Building the future of avionics safety

With technologies such as unmanned aerial drones and autonomous aircraft on the horizon, safety-critical technologies are becoming increasingly important to avionics applications. Intel remains committed to advancing avionics and defense industry technologies, and the Intel partnership with DDC-I has benefited many customers throughout these industries.

Intel® microprocessor technology, DDC-I's DO-178C DAL A-verified Deos RTOS, and the associated software life cycle data (certification baseline) together empower customers with the off-the-shelf solutions they need to build safety-critical programs. As a result, developers can concentrate on their own area of expertise when creating application software and the associated hardware, for solutions that perform optimally and differentiate them in the fast-advancing avionics marketplace.

About DDC-I

DDC-I offers complete solutions for embedded software developers, including field-proven safety-critical real-time embedded operating systems, multilanguage compilers, integrated development environments, runtime systems, [custom software development services](#), and legacy software system modernization solutions, with a primary focus on safety-critical applications.

ddci.com

Learn more

11th Gen Intel Core processors

Designed for avionics, defense, and other heavy-compute applications, 11th Gen Intel Core processors feature Intel® Time Coordinated Computing, functional safety design elements, extended temperature for cold and harsh environments, and long product availability on selected SKUs.³

[Get the details >](#)

Deos RTOS for Avionics

DDC-I's Deos RTOS solution enables multiple-core use on a microprocessor for time- and space-partitioned safety-critical computing. Deos has been verified for compliance with DO-178C/ED-12C Design Assurance Level A (DAL A) for avionics applications.

[Learn more >](#)



1. Source: https://www.ddci.com/products_deos_do_178c_arinc_653/

2. Source: Intel. Performance claim based on SPEC CPU 2017 metrics estimated by measurements on Intel® internal reference platforms completed on August 27, 2020. Graphics claim based on 3DMark11_V1.0.4 Graphics Score estimated by measurements on Intel internal reference platforms on August 27, 2020.

Testing configuration

Processor: Intel® Core™ i7 1185G7E PL1=15W TDP, 4C8T turbo up to 4.4 GHz

Graphics: Intel® Graphics Gen 12 gfx

Memory: 16 GB DDR4-3200

Storage: Intel® SSDPEKKW512GB (512 GB, PCIe 3.0 x4)

OS: Windows 10 Pro (x64) Build 19041.331 (2004/May 2020 update). Power policy set to AC/Balanced mode for all benchmarks. All benchmarks run in admin mode and Tamper Protection disabled/Defender disabled.

Bios: Intel Corporation TGLSFW11.R00.3333.A00.2008122042OneBKC: tgl_b2b0_up3_pv_up4_qs_ifwi_2020_ww32_4_01

Processor: Intel® Core™ i7 8665UE 15W PL1=15W TDP, 4C8T turbo up to 4.4 GHz

Graphics: Intel® Graphics Gen 9 gfx

Memory: 16 GB DDR4-2400

Storage: Intel® SSD 5455 (512 GB)

OS: Windows 10 Enterprise (x64) Build 18362.175 (1903/May 2019 update). Power policy set to AC/balanced mode for all benchmarks. All benchmarks run in Admin mode and Tamper Protection disabled/Defender disabled.

Bios: CNLSFW11.R00.X208.B00.1905301319

3. Not all features are available in all SKUs.

Notices and disclaimers

Performance varies by use, configuration, and other factors. Learn more at intel.com/PerformanceIndex.

Performance results are based on testing as of dates shown in configurations and may not reflect all publicly available updates. No product or component can be absolutely secure.

Intel® Advanced Vector Extensions (Intel® AVX) provides higher throughput to certain processor operations. Due to varying processor power characteristics, using Intel AVX instructions may cause, a) some parts to operate at less than the rated frequency and, b) some parts with Intel® Turbo Boost Technology 2.0 to not achieve any or maximum turbo frequencies. Performance varies depending on hardware, software, and system configuration, and you can learn more at intel.com/go/turbo.

Intel® processors of the same SKU may vary in frequency or power as a result of natural variability in the production process.

Not all features are available on all SKUs. Not all features are supported in every operating system.

Your costs and results may vary.

Intel® technologies may require enabled hardware, software, or service activation.

© Intel Corporation. Intel, the Intel logo, and other Intel marks are trademarks of Intel Corporation or its subsidiaries. Other names and brands may be claimed as the property of others.

1221/LM/CMD/PDF