Intel® Enpirion® Power Solutions: Intel Arria® 10 Power Solution Reference Design

REV	DATE	PAGES	DESCRIPTION
A	March 2017	All	Initial Release. This Reference Design demonstrates a complete power solution for a 30W core Intel® Arria® 10 FPGA or SoC FPGA design with complementary peripherals. This design is an upgraded variant of the power solution design used with Intel's Arria 10 SoC Development Kit. This solution is intended to provide a complete and validated Intel Arria 10 power solution, using Intel Enpirion® Power Solutions to achieve excellent power performance and high overall board power density. This schematics file includes the Arria 10 SoC Development Kit design with the following enhancements: - Intel Enpirion EM2130L01QI used to generate 3.3V IBC Power (pg 51) - Intel Enpirion EM2130L01QI used to generate Arria 10 VCC Core Power (pg 56) - Intel Enpirion ER2120QI used to generate 5V (pg 50) - J28 changed to the Enpirion Power Header (pg 45)

Learn more about the Intel Arria 10 SoC Development Kit at:
https://www.altera.com/products/boards_and_kits/dev-kits/altera/arria-10-soc-development-kit.html

Find additional design resources for Intel Arria 10 FPGAs at:
https://www.altera.com/products/fpga/arria-series/arria-10/support.html

Find additional design resources for Intel Arria 10 SoCs at:
https://www.altera.com/products/soc/portfolio/arria-10-soc/support.html

Find additional design resources for Intel Enpirion Power Solutions at:
www.altera.com/enpirion

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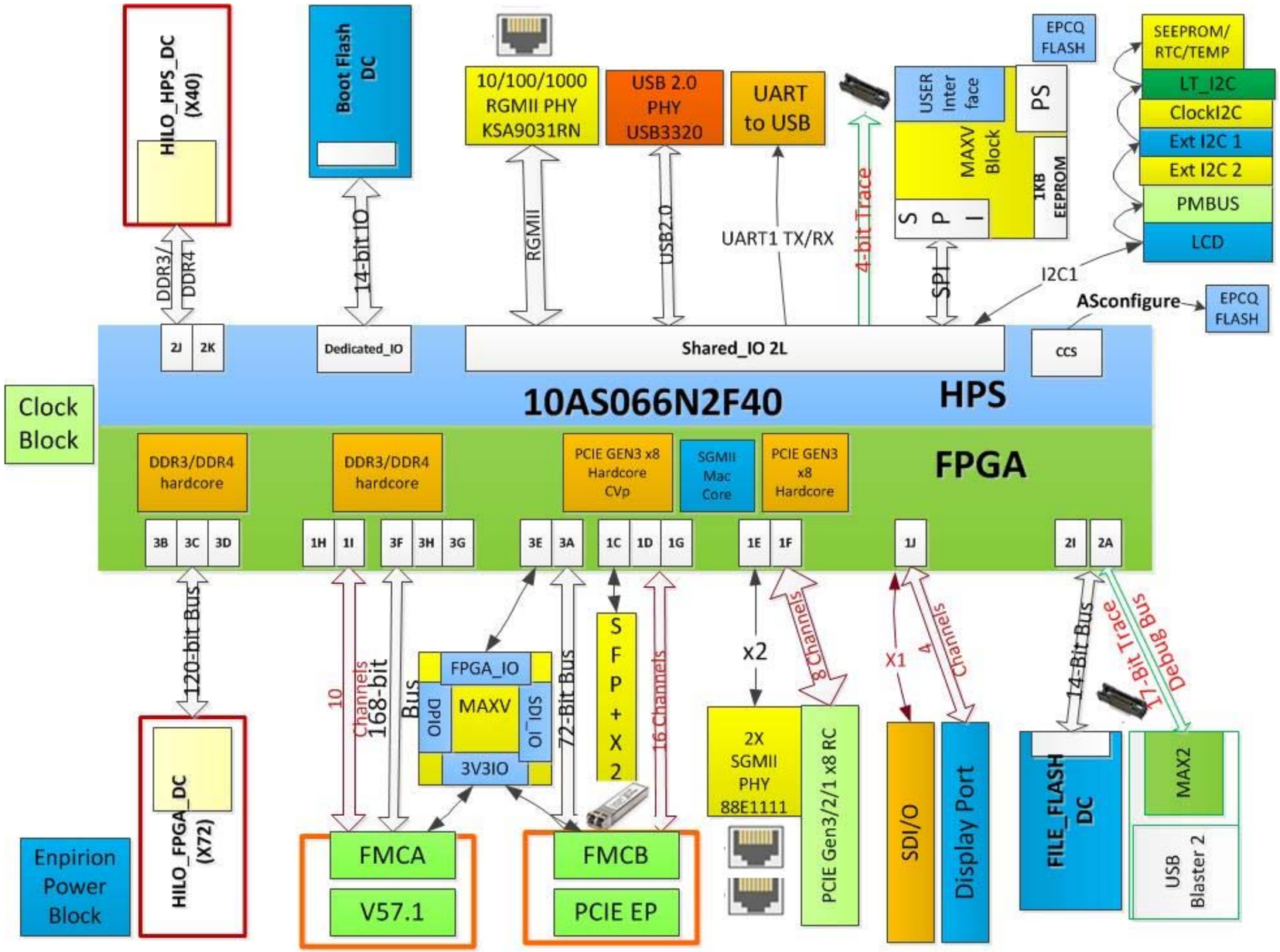
Reference Design Block Diagram

(Based on Intel® Arria® 10 SoC Development Kit)



V57.1 Two FMC Slots

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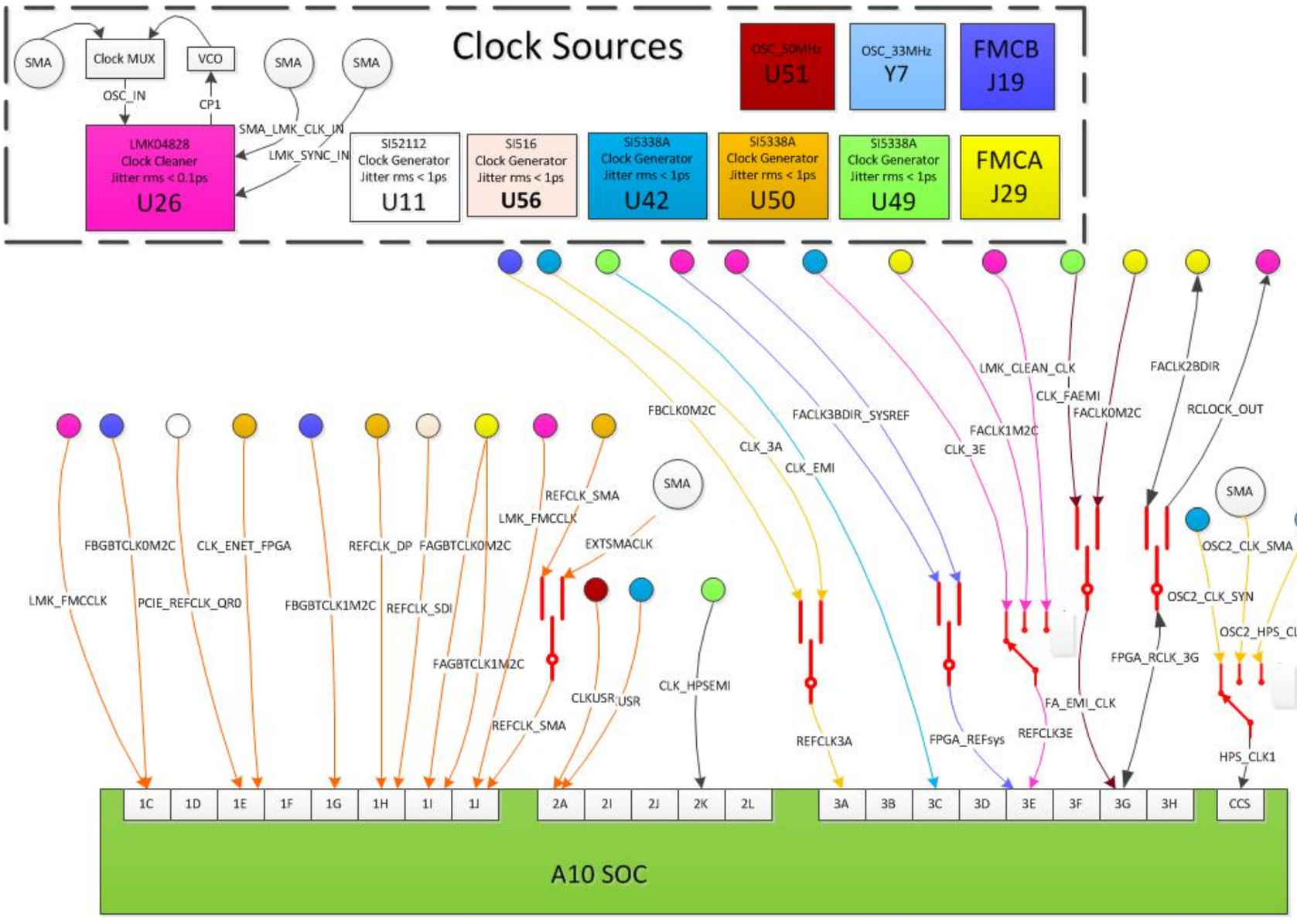
Reference Design Clock Connection

(Based on Intel® Arria® 10 SoC Development Kit)



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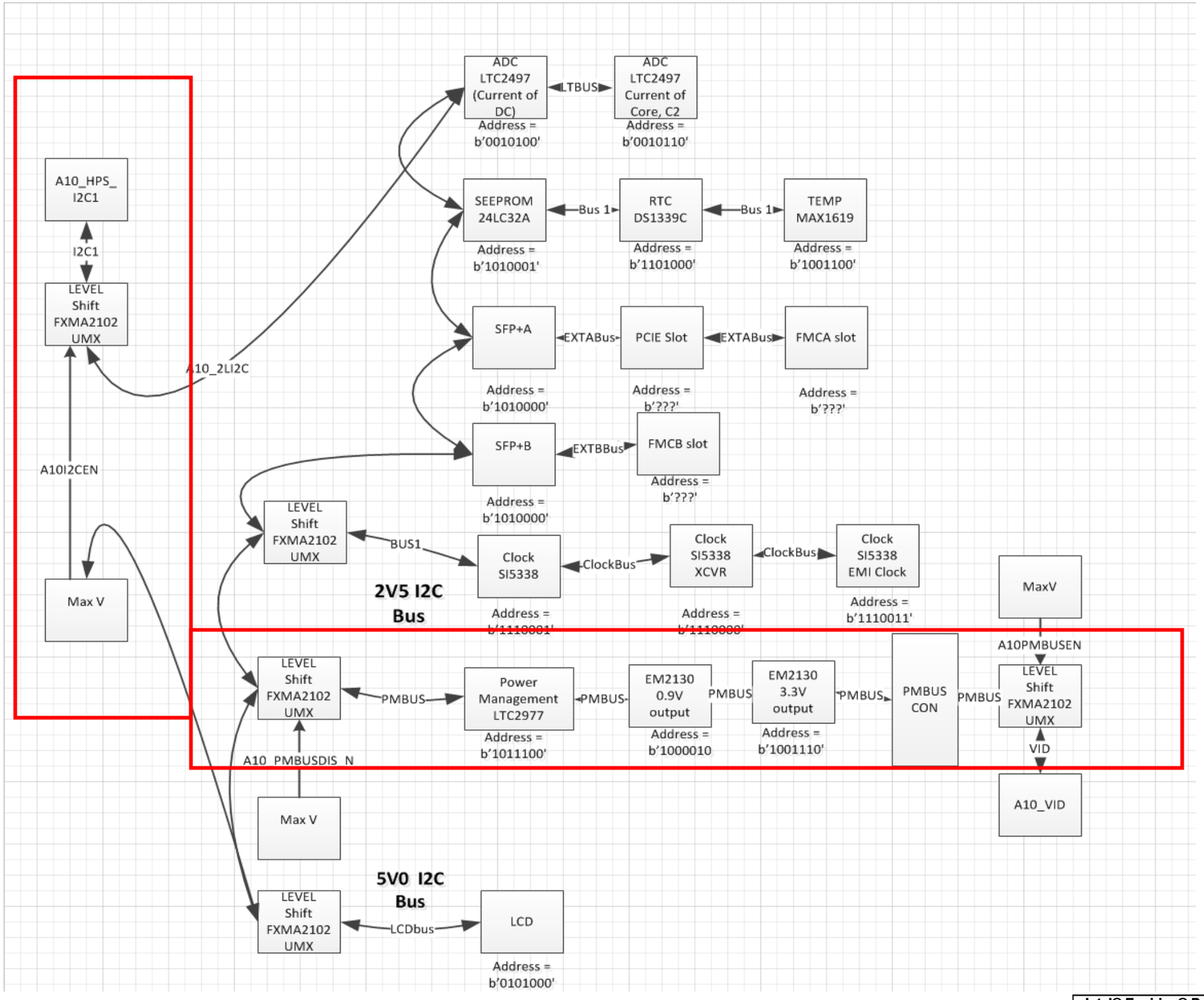
Reference Design I2C Bus Connection

(Based on Intel® Arria® 10 SoC Development Kit)



Application of two I2C masters in PMVID bus

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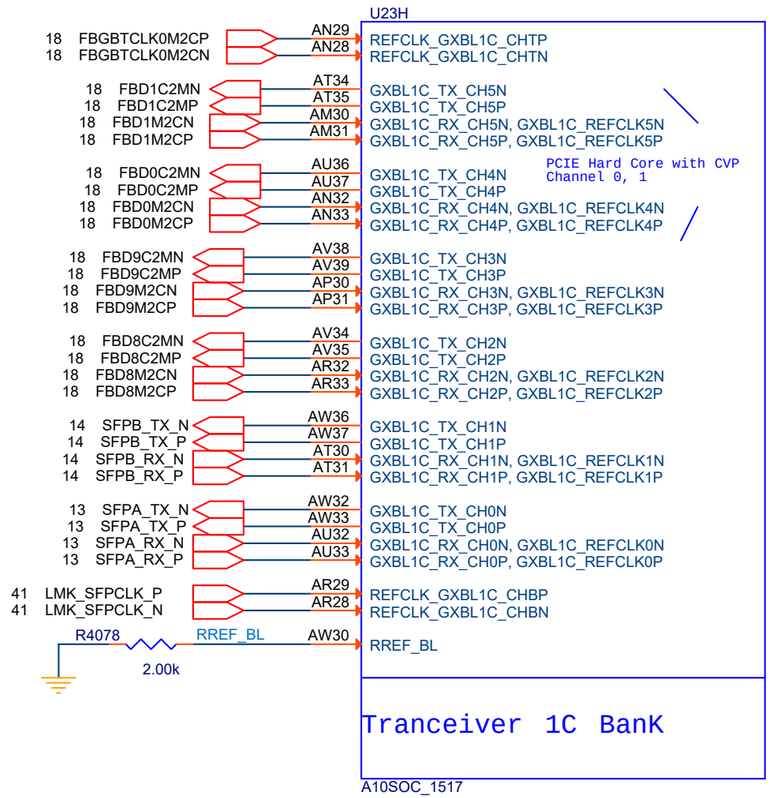
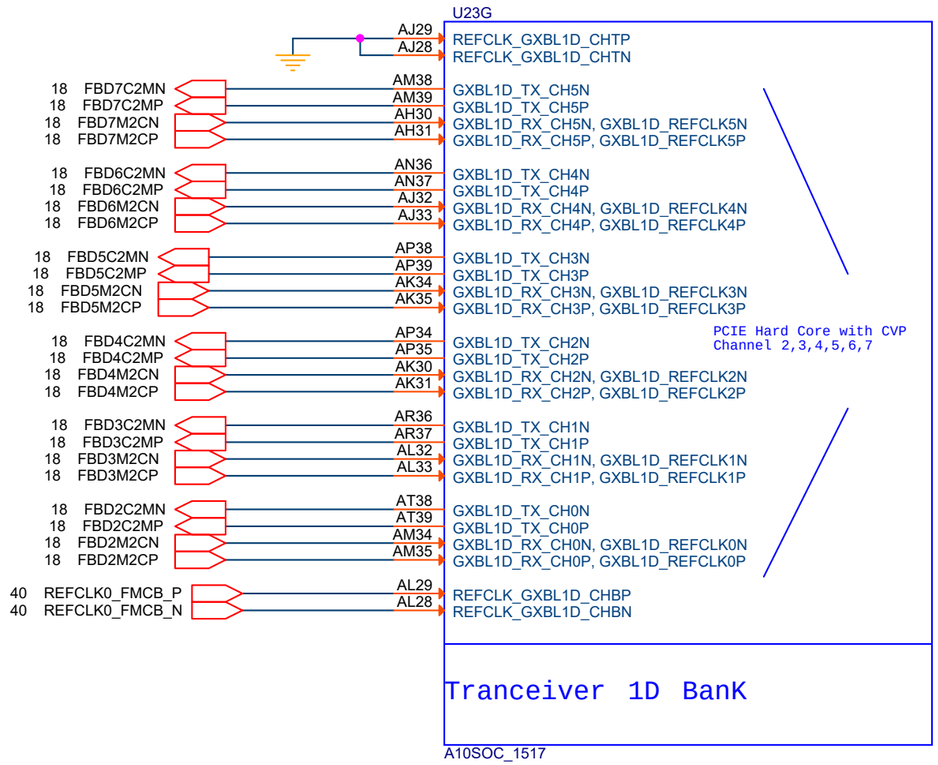
FMCB (PCIE END-POINT) XCVRs & 2 x SFP + XCVRs





Application	Channel (Bank, number)
PCIE EP	(1C,4);(1C,5);(1D,0);(1D,1); (1D,2);(1D,3);(1D,4);(1D,5)
FMC B Slot DP Transceiver [0:9]	(1C,2);(1C,3);(1C,4);(1C,5); (1D,0);(1D,1);(1D,2);(1D,3); (1D,4);(1D,5);
SFP+ 0 and 1	(1C,0);(1C,1)

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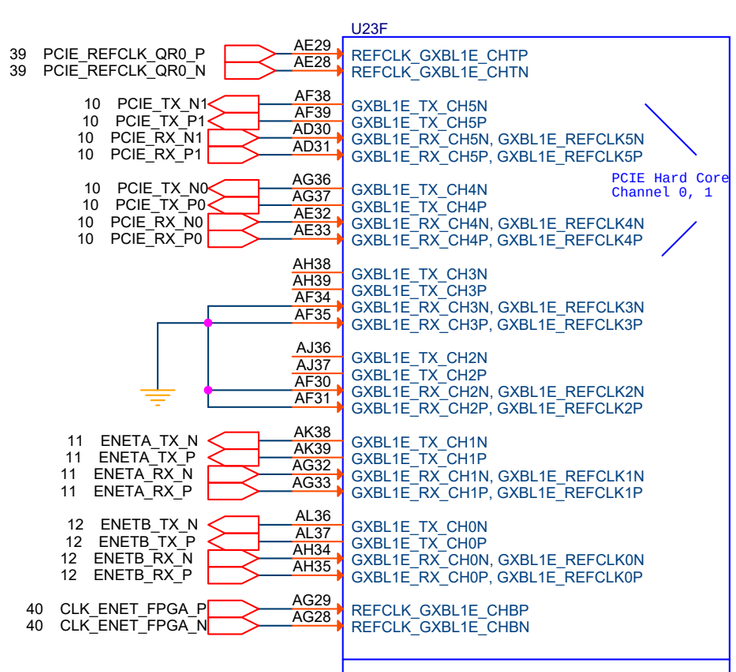
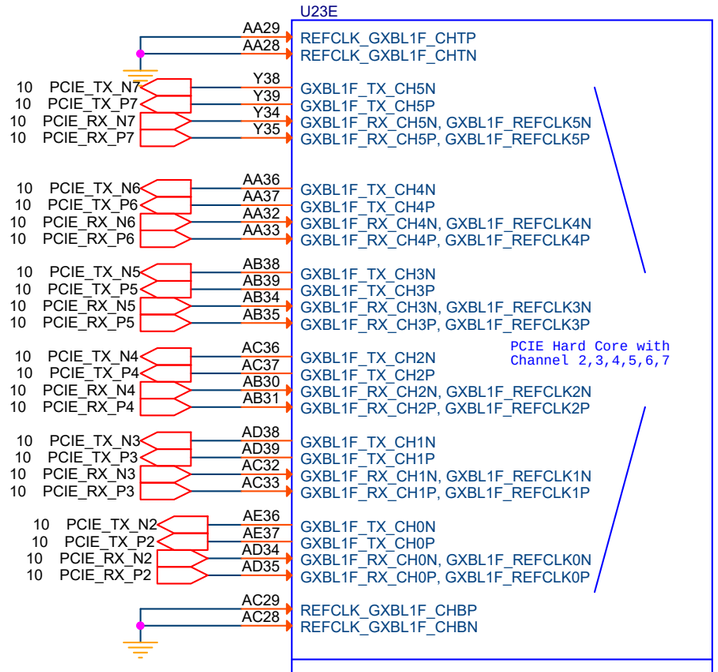
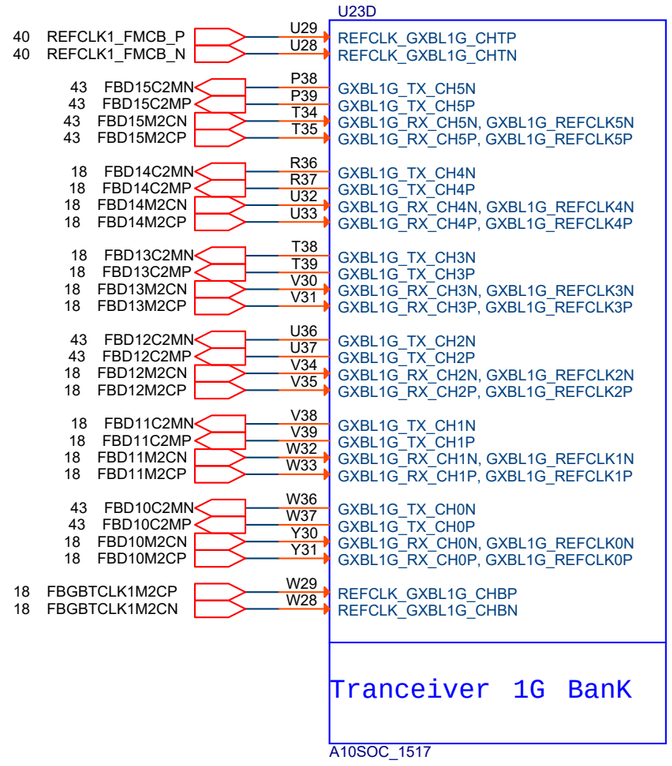
PCIE RC XCVRs & 2X SGMII XCVRs & FMCB XCVRs







Application	Channel (Bank, number)
PCIE RC	(1E,4);(1E,5);(1F,0);(1F,1); (1F,2);(1F,3);(1F,4);(1F,5)
FMC B Slot DP Transceiver [10:15]	(1G,0);(1G,1);(1G,2);(1G,3); (1G,4);(1G,5);
SGMII A and B	(1E,0);(1E,1)

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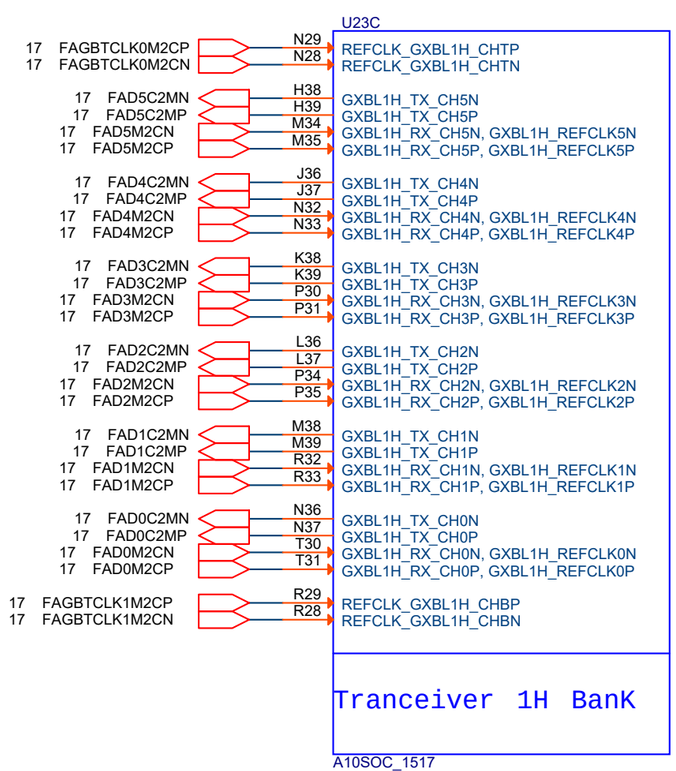
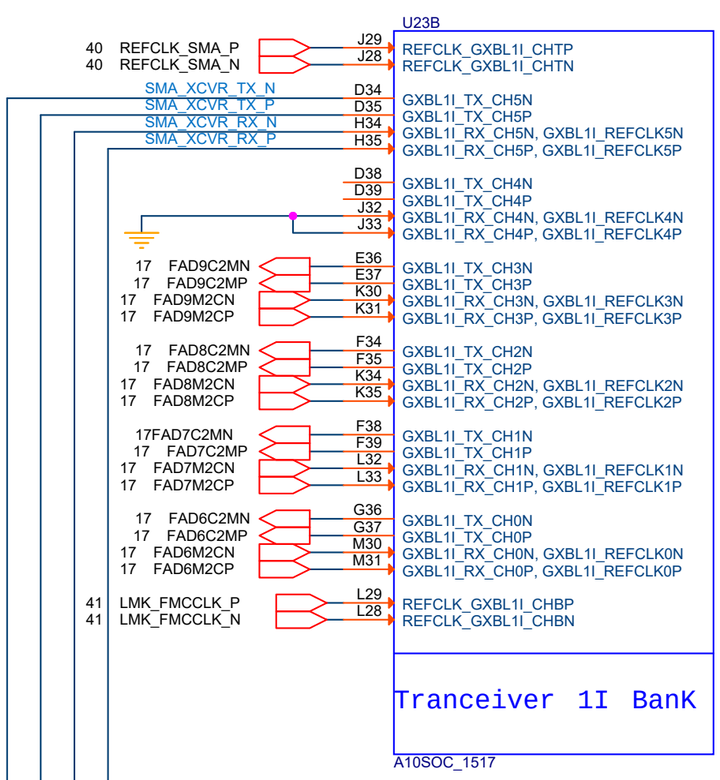
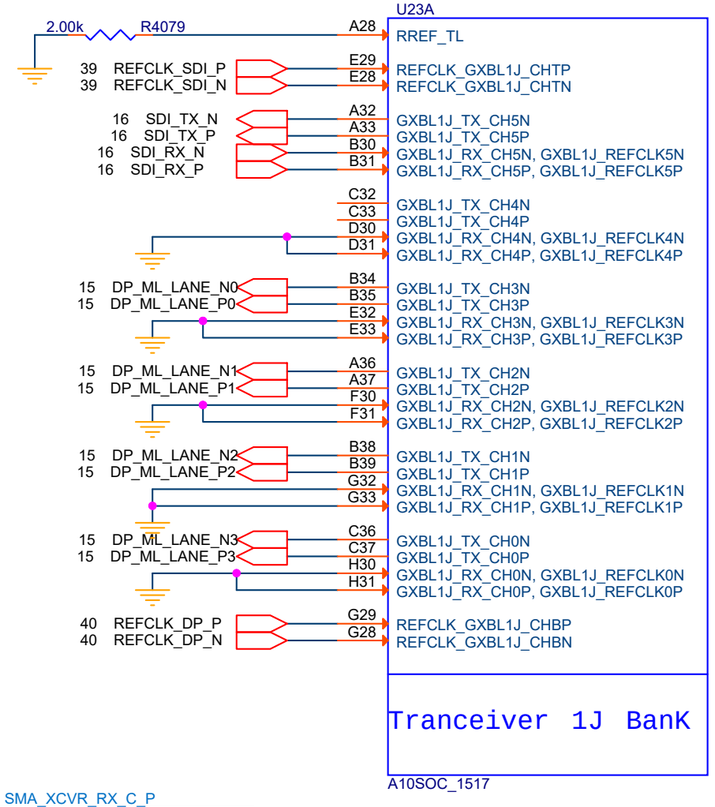
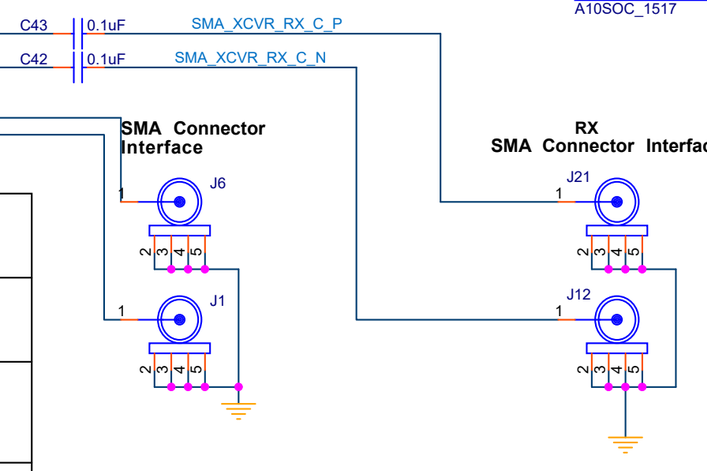
DP & SDI & FMCA XCVRs & SMA XCVR









Application	Channel (Bank, number)
SMA	(1I,5)
FMC A Slot DP Transceiver [0:9]	(1H,0);(1H,1);(1H,2);(1H,3]; (1H,4);(1H,5);(1I,0);(1I,1); (1I,2);(1I,3);
SDI	(1J,5)
Display Port	(1J,0);(1J,1);(1J,2);(1J,3)

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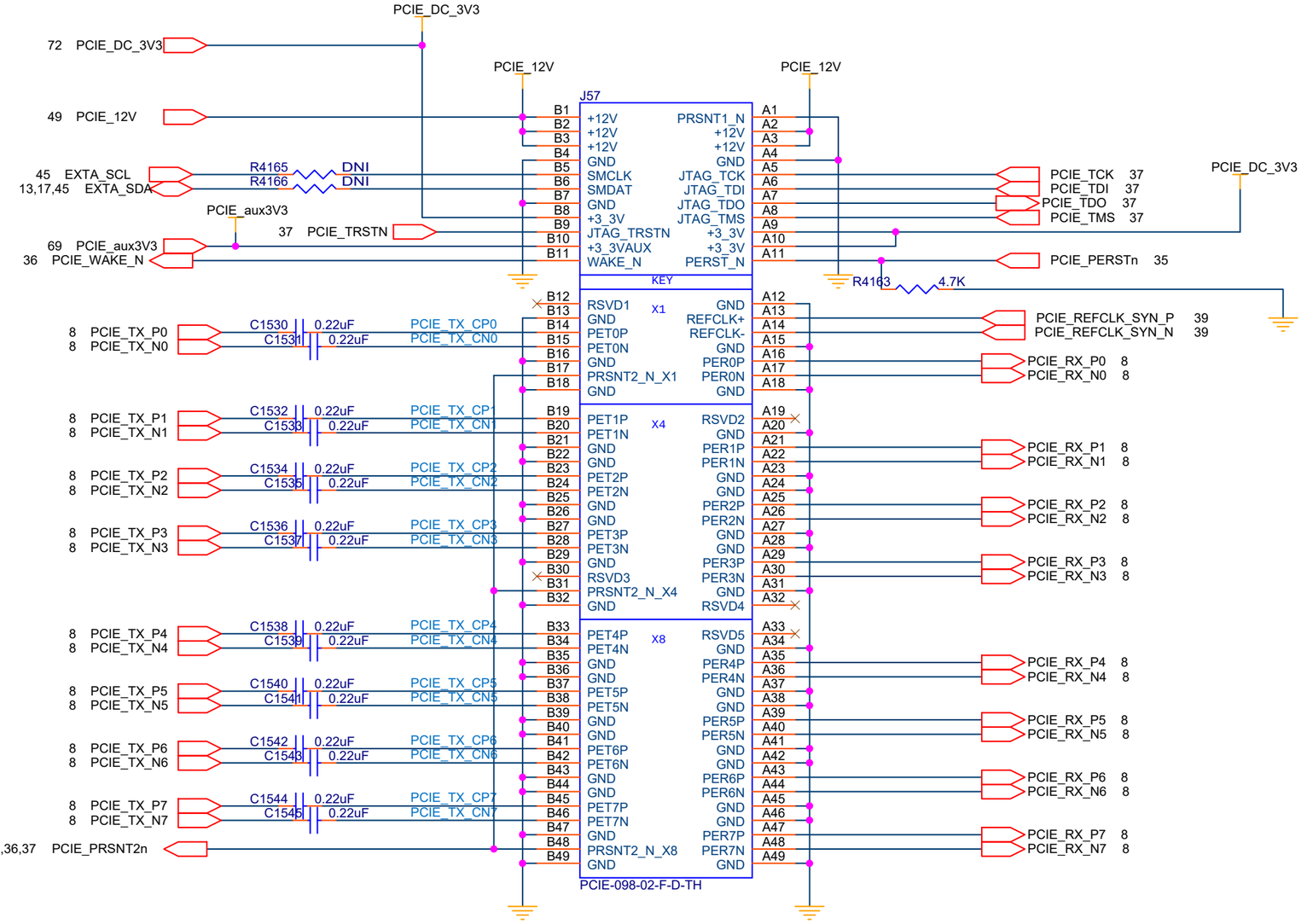
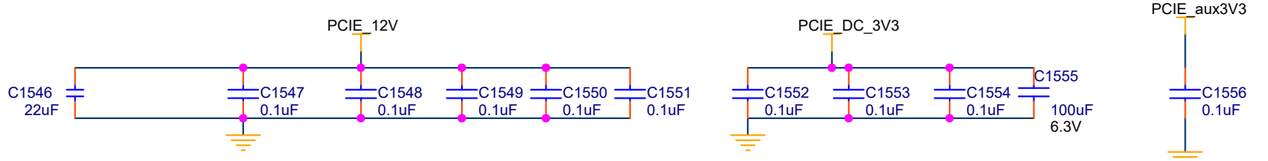
PCI Express GEN3 X 8 Connector



75-ohm to 100-ohm XCVR traces.



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10/100/1000 Ethernet XCVR

Pin	Pin Connection	Setting Bit[2:0]	Definition
CONFIG0	GND	000	MDIO PHY Address bit (2:0) = 000
CONFIG1	GND	000	Enable Pause, PHY Address bits (4:3) = 00
CONFIG2	VDDO (2.5V or 3.3V)	111	1110 = Auto-negotiate, advertise all capabilities, prefer Master 100BASE-x FULL-DUPLEX/Auto-Negotiation enabled, 100BASE-X half-duplex
CONFIG3	GND	000	Disable crossover, Enable 125CLK
CONFIG4	LED_LINK1000	100	Hardware Config Mode Reg (2:0) = 100 SGMII without Clock with SGMII Auto-Neg to copper
CONFIG5	LED_LIN10	110	Disable fiber/copper autosel, disable sleep mode (enable energy detect), Hardware Config Mode Reg (3) = 0
CONFIG6	LED_RX	010	Select MDIO (over 2-wire serial), interrupt polarity = active low, 50-ohm termination for fiber

SGMII Mode (default)

88E1111-B2-CAA1C000 EOL
88E1111-B2-NDC2C000 Replacement

ENET_DVDD = 1.0V/0.207A

DVDD = 1.0V
DVDD = 1.2V

Place near 88E1111 PHY

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10/100/1000 Ethernet XCVR

Pin	Pin Connection	Setting Bit[2:0]	Definition
CONFIG0	GND	000	MDIO PHY Address bit (2:0) = 000
CONFIG1	GND	000	Enable Pause, PHY Address bits (4:3) = 00
CONFIG2	VDDO (2.5V or 3.3V)	111	1110 = Auto-negotiate, advertise all capabilities, prefer Master 100BASE-x FULL-DUPLEX/Auto-Negotiation enabled, 100BASE-X half-duplex
CONFIG3	GND	000	Disable crossover, Enable 125CLK
CONFIG4	LED_LINK1000	100	Hardware Config Mode Reg (2:0) = 100 SGMII without Clock with SGMII Auto-Neg to copper
CONFIG5	LED_LIN10	110	Disable fiber/copper autosel, disable sleep mode (enable energy detect), Hardware Config Mode Reg (3) = 0
CONFIG6	LED_RX	010	Select MDIO (over 2-wire serial), interrupt polarity = active low, 50-ohm termination for fiber

88E1111-B2-CAA1C000 EOL
88E1111-B2-NDC2C000 Replacement

Place near 88E1111 PHY

SGMII Mode (default)

DVDD = 1.0V
DVDD = 1.2V

ENET_DVDD = 1.0V/0.207A

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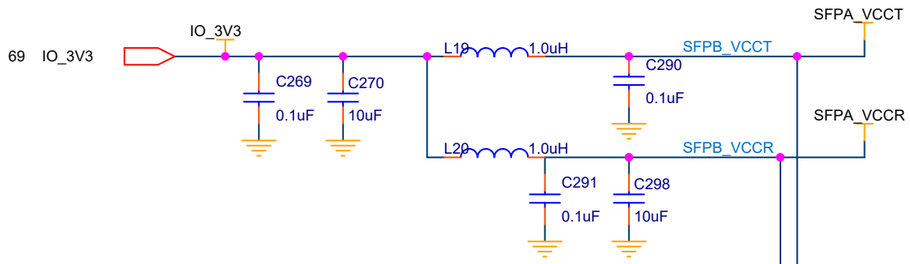
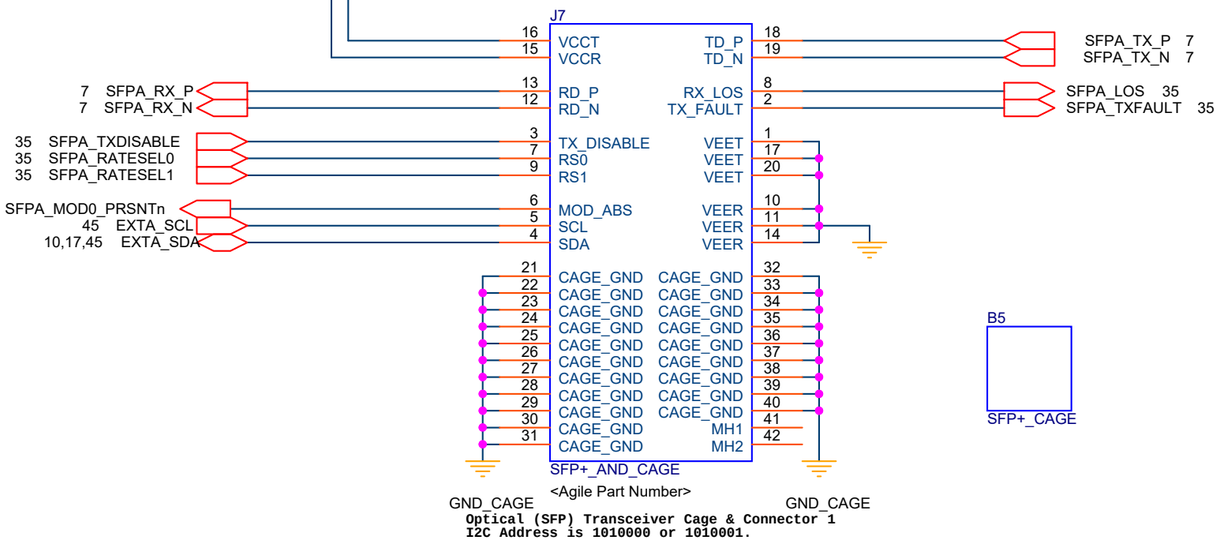
Small Form Factor Pluggable Plus (SFP+) Port A



Optical (SFP+) Transceiver Cage & Connector 0



Optical (SFP) Transceiver Cage & Connector 1
I2C Address is 1010000 or 1010001.

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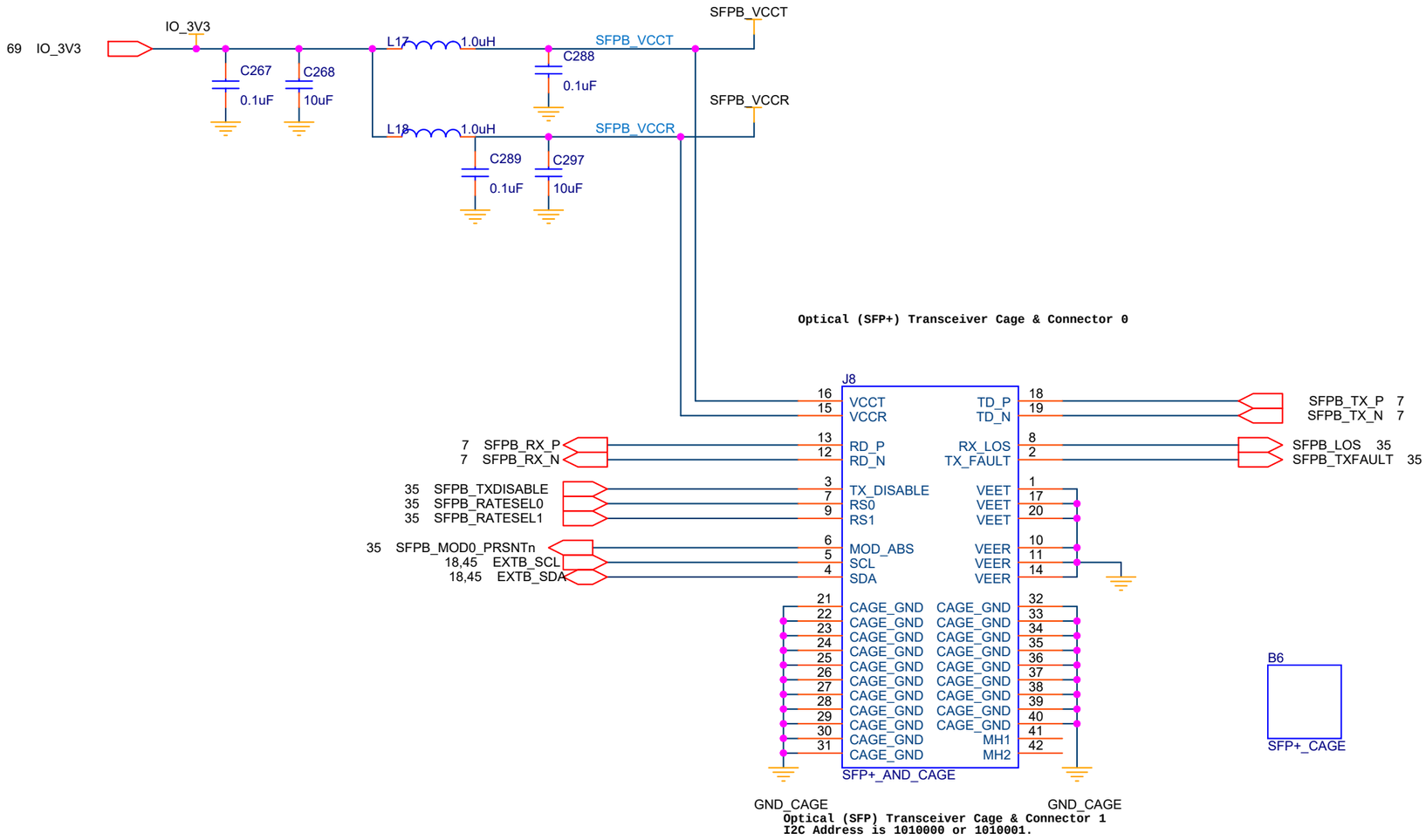
Small Form Factor Pluggable Plus (SFP+) Port B



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Display Port (x4)

1) TX uses diff sstl18 configuration, which is able to meet peak-to-peak differential voltage and common mode voltage spec for DP.
2) RX uses LVDS input, but user need to ensure pin voltage at NF receiver end is <1.9v.
   a. If the channel is AC couple, then user need to choose the correct Vbias_RX so that Vpin < 1.9v. The spec is 0 – 2v, which is quite wide. Selecting Vbias_Rx at 2v region will cause NF device to have reliability issue.
   b. If the channel is DC couple, user need to make sure TX common mode voltage + ground reference differences between Tx and Rx will not cause Vpin for NF to be higher than 1.9v.

IO_3V3 R806 100K C893 2.2uF U71 MAX14523B (IN, NC1, NC2, FLAG, ON, OUT, SETI, GND, GND_PAD) DP_3V3 R802 280K 1% C888 0.1uF
0.5A maximum current
36 DP_OCn
36 DP_ON

DP_3V3 C134 0.1uF C133 0.1uF D38 D37 82401646 (VDD, GND, IO6, IO5, IO1, IO2, IO3, IO4)

DP_3V3 J46 0472720024 (DP_PWR, HP_DETECT, RTN, CONFIG1, CONFIG2, GND, MH1, MH2, ML_LANE_0P/N, ML_LANE_1P/N, ML_LANE_2P/N, ML_LANE_3P/N, AUX_CH_P/N, MH3, MH4)
R792 100K DP_HOT_PLUG
DP_RTN R793 0
R790 1M DP_3p3V_CONFIG1
R791 1M DP_3p3V_CONFIG2
36 DP_CONFIG1
36 DP_CONFIG2
1M R765 4.7nF C878 GND_DP
GND_DP GND_DP
36 DP_HOT_PLUG

DP_ML_LANE_CP0 DP_ML_LANE_CN0 C854 0.1uF C855 0.1uF DP_ML_LANE_P0 DP_ML_LANE_N0
DP_ML_LANE_CP1 DP_ML_LANE_CN1 C856 0.1uF C857 0.1uF DP_ML_LANE_P1 DP_ML_LANE_N1
DP_ML_LANE_CP2 DP_ML_LANE_CN2 C858 0.1uF C859 0.1uF DP_ML_LANE_P2 DP_ML_LANE_N2
DP_ML_LANE_CP3 DP_ML_LANE_CN3 C860 0.1uF C2453 0.1uF DP_ML_LANE_P3 DP_ML_LANE_N3
DP_ML_LANE_P0 9 DP_ML_LANE_N0 9
DP_ML_LANE_P1 9 DP_ML_LANE_N1 9
DP_ML_LANE_P2 9 DP_ML_LANE_N2 9
DP_ML_LANE_P3 9 DP_ML_LANE_N3 9

DP_AUX_CP DP_AUX_CN Auxilary Channel -> Bidirctional LVDS 1Mbps/(720Mbps optional).

Quartus IO Standard = BLVDS
TX -> DIFF SSTL-1.8
RX -> LVDS
FogBugz Case 135234 & 147387

IO_1V8 IO_3V3
Usually 3.3V for DP, but Arria 10 is 1.8V LVDS.
R223 10K R750 DNI
C848 10uF C847 0.1uF R220 10K
VBIAS_DP

DP_AUX_CP C137 0.1uF R224 100K R216 49.9
DP_3V3 R225 100K C138 0.1uF R219 49.9
DP_AUX_CHR_P DP_AUX_CHR_N R217 22.0 R218 22.0 DP_AUX_CH_P 27 DP_AUX_CH_N 27
DNI R211 DNI R212
DP_AUX_CHB_P DP_AUX_CHB_N

U28 TPD2EUSB30 (D+, D-, GND)

U27 DNI (DE, D, RE_n, R, A, B, VCC, GND)
IO_3V3 C830 0.1uF

IO_1V8 IO_3V3
IO_1V8 36,37,68
IO_3V3 69
DP_AUX_DE 36
DP_AUX_D 36
DP_AUX_REn 36
DP_AUX_R 36

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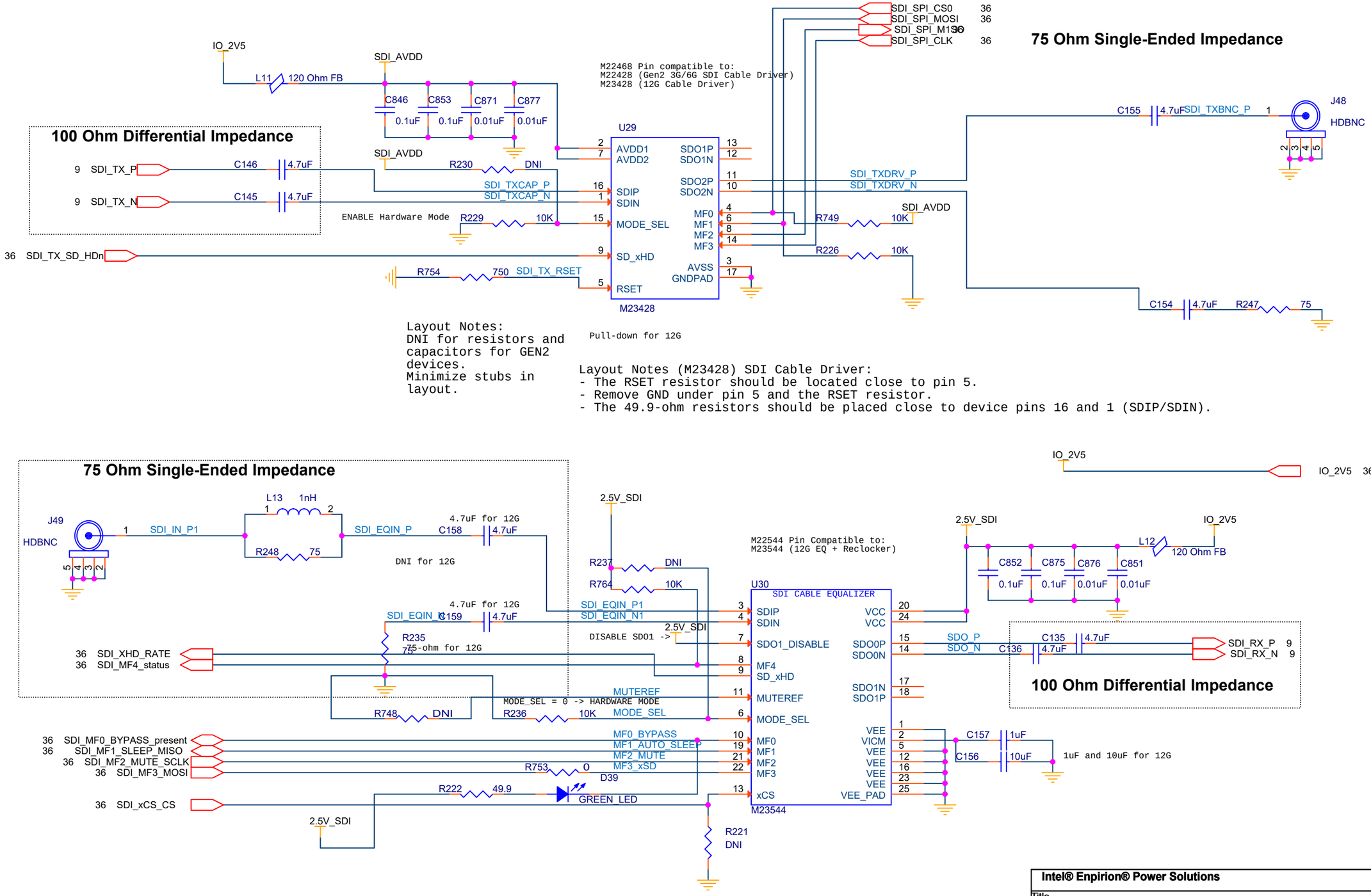
SDI Cable Driver, Equalizer, and SMB



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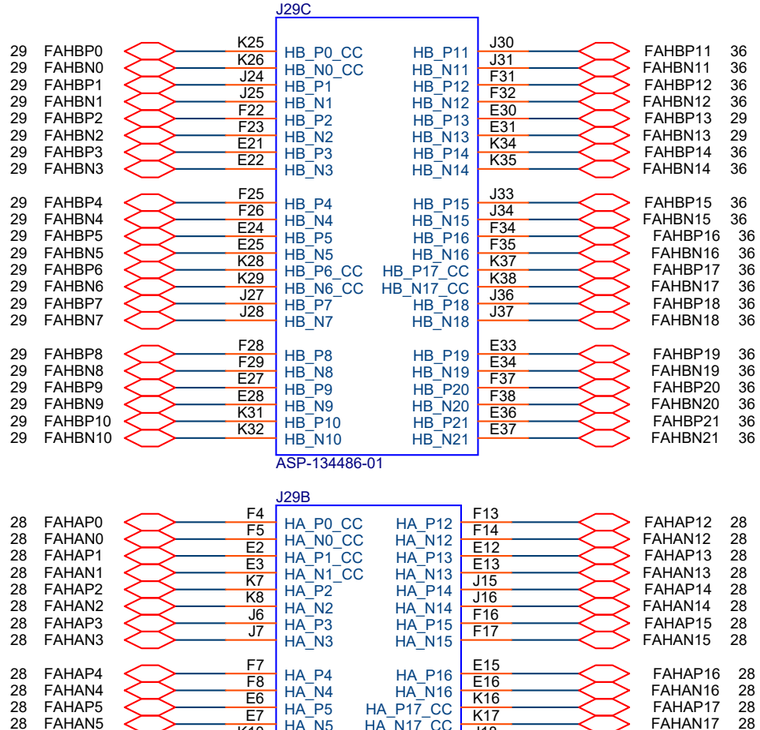
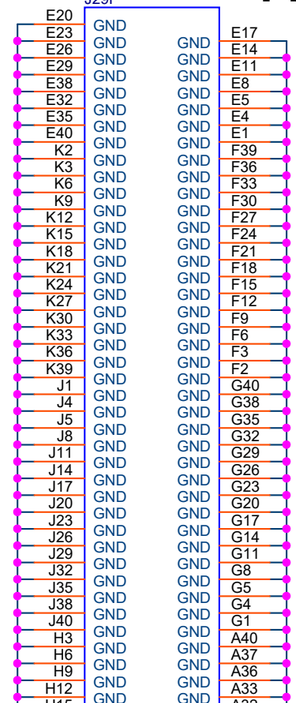
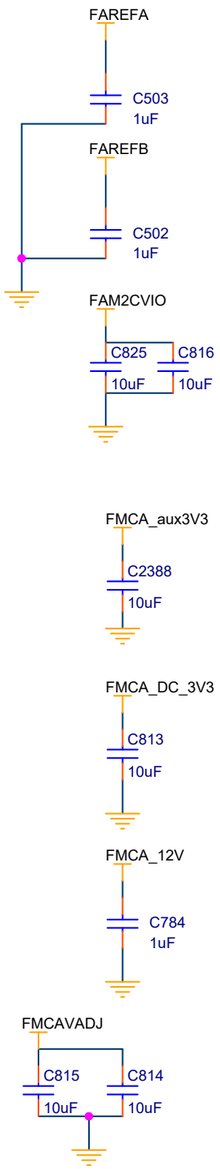
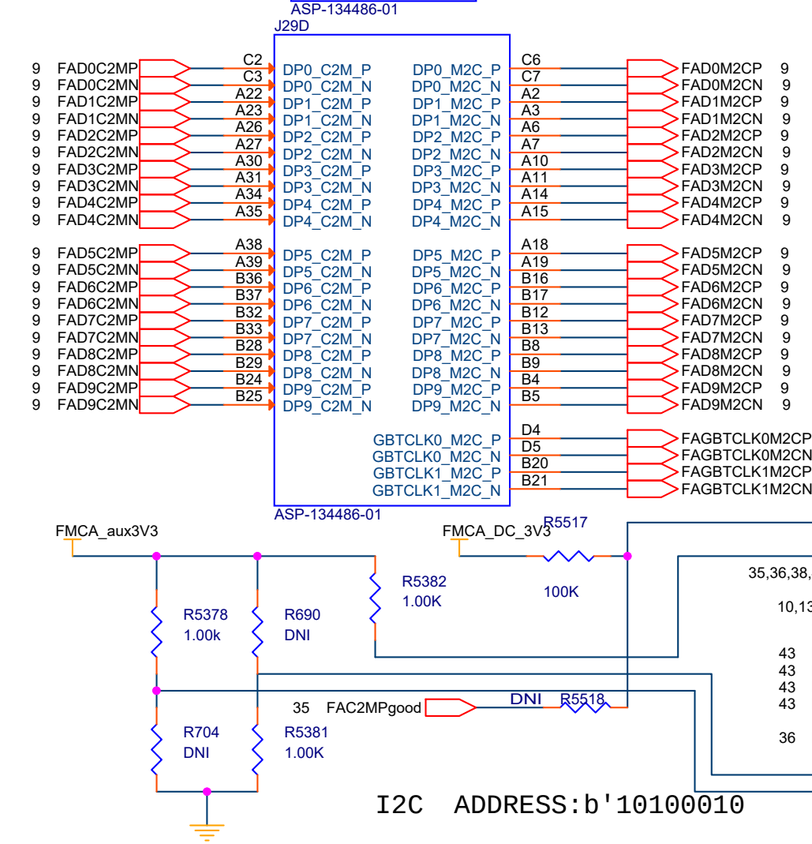
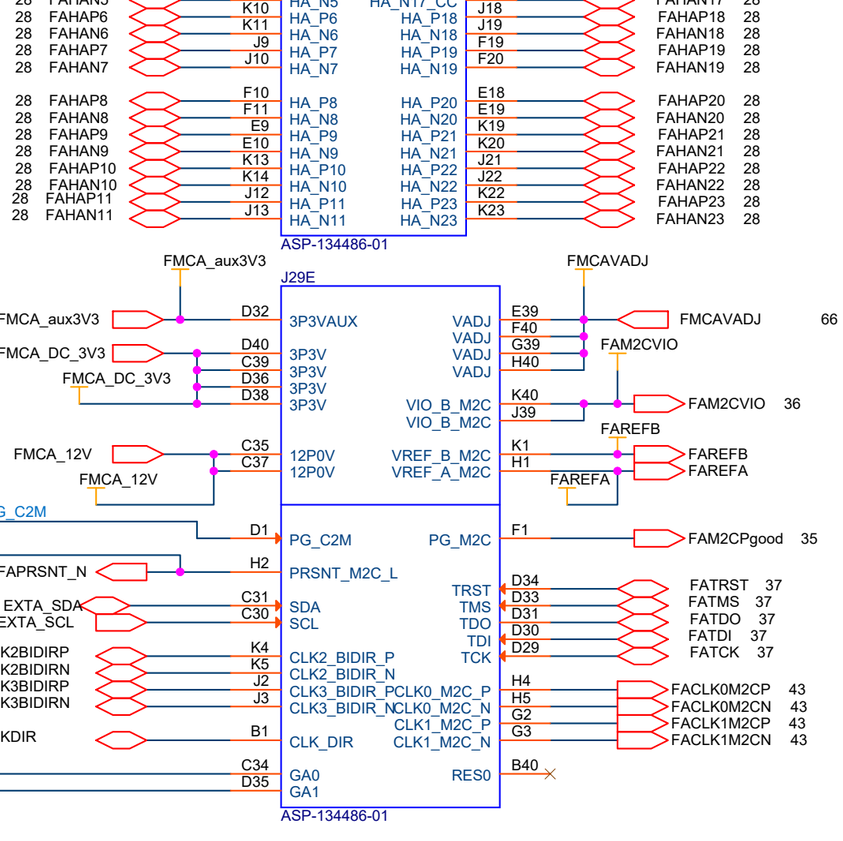
FMC (V57.1) PORT A











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FMC (16 XCVRS + LAP) PORT B

J19A
ASP-134486-01
J19C
ASP-134486-01
J19B
ASP-134486-01
J19F
ASP-134486-01
J19D
ASP-134486-01
J19E
ASP-134486-01

FMCBVADJ
C446 10uF
C447 10uF
FBREFA
C238 1uF
FMCB_aux3V3
C405 10uF
FMCB_DC_3V3
C434 10uF
FMCB_12V
C424 1uF
FBM2CVIO
C466 10uF
C448 10uF

R5359 1.00k
R5355 1.00k
R457 DNI
R5519 100K
R464 DNI
R5358 1.00k
R5520 DNI

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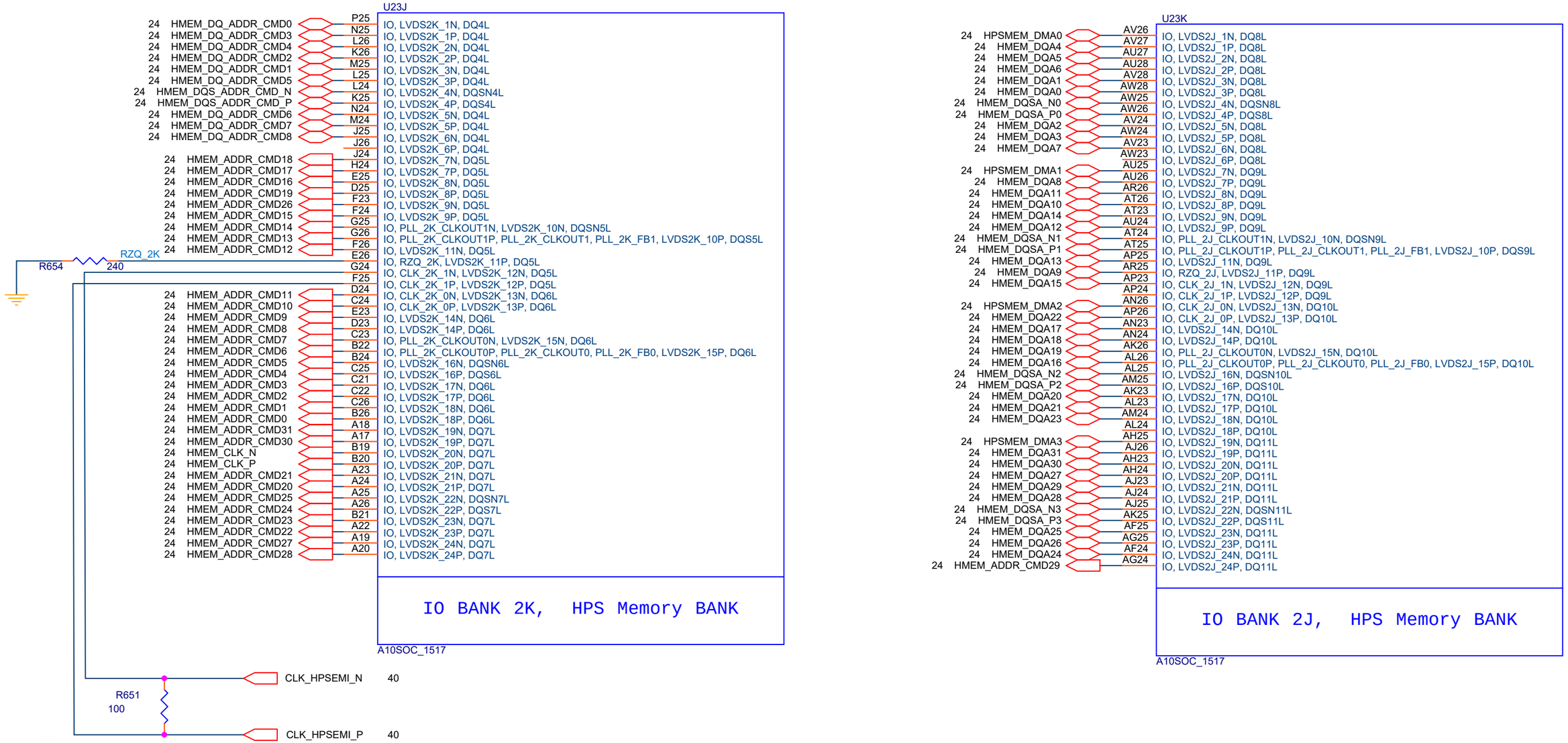
HPS HILO DDR3/DDR4 IOs



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All HPS memory IO pin assignment must be same as Quartus'

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HPS Shared IOs

U23I

25 USB_CLK	D18	IO, DQ0L, GPIO0_IO0,NAND_ADQ0,UART0_CTS_N,USB0_CLK,SDMMC_DATA0,SPIM0_SS1_N,SPIS0_CLK
25 USB_STP	E18	IO, DQ0L, GPIO0_IO1,NAND_ADQ1,UART0_RTS_N,USB0_STP,SDMMC_CMD,SPIM1_SS1_N,SPIS0_MOSI
25 USB_DIR	C19	IO, DQ0L, GPIO0_IO2,NAND_WE_N,UART0_TX,USB0_DIR,SDMMC_CCLK,SPIS0_SS0_N,I2C1_SDA
25 USB_DATA0	D19	IO, DQ0L, GPIO0_IO3,NAND_RE_N,UART0_RX,USB0_DATA0,SDMMC_DATA1,SPIS0_MISO,I2C1_SCL
25 USB_DATA1	E17	IO, DQ0L, GPIO0_IO4,NAND_WP_N,UART1_CTS_N,QSPI_SS2,USB0_DATA1,SDMMC_DATA2,SPIM0_CLK,I2C0_SDA
25 USB_NXT	F17	IO, DQ0L, GPIO0_IO5,NAND_ADQ2,UART1_RTS_N,QSPI_SS3,USB0_NXT,SDMMC_DATA3,SPIM0_MOSI,I2C0_SCL
25 USB_DATA2	C17	IO, DQSN0L, GPIO0_IO6,NAND_ADQ3,UART1_TX,USB0_DATA2,SDMMC_DATA4,SPIM0_MISO,EMAC2_MDIO,I2C_EMAC2_SDA
25 USB_DATA3	C18	IO, DQS0L, GPIO0_IO7,NAND_CLE,UART1_RX,USB0_DATA3,SDMMC_DATA5,SPIM0_SS0_N,EMAC2_MDC,I2C_EMAC2_SCL
25 USB_DATA4	D21	IO, DQ0L, GPIO0_IO8,NAND_ADQ4,USB0_DATA4,SDMMC_DATA6,SPIM1_CLK,SPIS1_CLK,EMAC1_MDIO,I2C_EMAC1_SDA
25 USB_DATA5	D20	IO, DQ0L, GPIO0_IO9,NAND_ADQ5,USB0_DATA5,SDMMC_DATA7,SPIM1_MOSI,SPIS1_MOSI,EMAC1_MDC,I2C_EMAC1_SCL
25 USB_DATA6	E21	IO, DQ0L, GPIO0_IO10,NAND_ADQ6,USB0_DATA6,SPIM1_MISO,SPIS1_SS0_N,EMAC0_MDIO,I2C_EMAC0_SDA
25 USB_DATA7	E22	IO, DQ0L, GPIO0_IO11,NAND_ADQ7,USB0_DATA7,SPIM1_SS0_N,SPIS1_MISO,EMAC0_MDC,I2C_EMAC0_SCL
22 ENET_HPS_GTX_CLK	H18	IO, DQ1L, GPIO0_IO12,NAND_ALE,USB1_CLK,EMAC0_TX_CLK
22 ENET_HPS_TX_EN	H19	IO, DQ1L, GPIO0_IO13,NAND_RB,USB1_STP,EMAC0_TX_CTL
22 ENET_HPS_RX_CLK	F18	IO, DQ1L, GPIO0_IO14,NAND_CE_N,USB1_DIR,EMAC0_RX_CLK
22 ENET_HPS_RX_DV	G17	IO, DQ1L, GPIO0_IO15,USB1_DATA0,EMAC0_RX_CTL
22 ENET_HPS_TXD0	E20	IO, DQ1L, GPIO0_IO16,NAND_ADQ8,USB1_DATA1,EMAC0_TXD0
22 ENET_HPS_TXD1	F20	IO, DQ1L, GPIO0_IO17,NAND_ADQ9,USB1_NXT,EMAC0_TXD1
22 ENET_HPS_RXD0	G20	IO, PLL_2L_CLKOUT1N, DQSN1L, GPIO0_IO18,NAND_ADQ10,USB1_DATA2,EMAC0_RXD0
22 ENET_HPS_RXD1	G21	IO, PLL_2L_CLKOUT1P, PLL_2L_CLKOUT1, PLL_2L_FB1, DQS1L, GPIO0_IO19,NAND_ADQ11,USB1_DATA3,EMAC0_RXD1,SPIM1_SS1_N
22 ENET_HPS_TXD2	F19	IO, DQ1L, GPIO0_IO20,NAND_ADQ12,UART0_CTS_N,USB1_DATA4,EMAC0_TXD2,SPIM1_CLK,SPIS0_CLK,I2C1_SDA
22 ENET_HPS_TXD3	G19	IO, RZQ_2L, DQ1L, GPIO0_IO21,NAND_ADQ13,UART0_RTS_N,USB1_DATA5,EMAC0_TXD3,SPIM1_MOSI,SPIS0_MOSI,I2C1_SCL
22 ENET_HPS_RXD2	F22	IO, CLK_2L_1N, DQ1L, GPIO0_IO22,NAND_ADQ14,UART0_TX,USB1_DATA6,EMAC0_RXD2,SPIM1_MISO,SPIS0_SS0_N,I2C0_SDA
22 ENET_HPS_RXD3	G22	IO, CLK_2L_1P, DQ1L, GPIO0_IO23,NAND_ADQ15,UART0_RX,USB1_DATA7,EMAC0_RXD3,SPIM1_SS0_N,SPIS0_MISO,I2C0_SCL
35 SPIM1_CLK	K18	IO, CLK_2L_0N, DQ2L, GPIO1_IO0,NAND_ADQ0,UART0_CTS_N,EMAC1_TX_CLK,SPIM1_CLK
35 SPIM1_MOSI	L19	IO, CLK_2L_0P, DQ2L, GPIO1_IO1,NAND_ADQ1,UART0_RTS_N,EMAC1_TX_CTL,SPIM1_MOSI
35 SPIM1_MISO	H22	IO, DQ2L, GPIO1_IO2,NAND_WE_N,UART0_TX,EMAC1_RX_CLK,SPIM1_MISO,I2C0_SDA
35 SPIM1_SS0_N	H21	IO, DQ2L, GPIO1_IO3,NAND_RE_N,UART0_RX,EMAC1_RX_CTL,SPIM1_SS0_N,I2C0_SCL
35 SPIM1_SS1_N	J21	IO, PLL_2L_CLKOUT0N, DQ2L, GPIO1_IO4,NAND_WP_N,UART1_CTS_N,EMAC1_TXD0,SPIM1_SS1_N,SPIS1_CLK
35 A10SH_GPIO0	J20	IO, PLL_2L_CLKOUT0P, PLL_2L_CLKOUT0, PLL_2L_FB0, DQ2L, GPIO1_IO5,NAND_ADQ2,UART1_RTS_N,EMAC1_TXD1,SPIS1_MOSI
35 HPSUARTA_TX	J18	IO, DQSN2L, GPIO1_IO6,NAND_ADQ3,UART1_TX,EMAC1_RXD0,SPIS1_SS0_N,I2C1_SDA
35 HPSUARTA_RX	J19	IO, DQS2L, GPIO1_IO7,NAND_CLE,UART1_RX,EMAC1_RXD1,SPIS1_MISO,I2C1_SCL
42 USER_PB_HPS3	H23	IO, DQ2L, GPIO1_IO8,NAND_ADQ4,EMAC1_TXD2,SPIS0_CLK,EMAC2_MDIO,I2C_EMAC2_SDA
42 USER_DIPSW_HPS3	J23	IO, DQ2L, GPIO1_IO9,NAND_ADQ5,EMAC1_TXD3,SPIS0_MOSI,EMAC2_MDC,I2C_EMAC2_SCL
22 ENET_HPS_MDIO	K21	IO, DQ2L, GPIO1_IO10,NAND_ADQ6,EMAC1_RXD2,SPIS0_SS0_N,EMAC0_MDIO,I2C_EMAC0_SDA
22 ENET_HPS_MDC	K20	IO, DQ2L, GPIO1_IO11,NAND_ADQ7,EMAC1_RXD3,SPIS0_MISO,EMAC0_MDC,I2C_EMAC0_SCL
SH_SDA	L20	IO, DQ3L, GPIO1_IO12,NAND_ALE,EMAC2_TX_CLK,SDMMC_DATA0,I2C1_SDA
SH_SCL	M20	IO, DQ3L, GPIO1_IO13,NAND_RB,EMAC2_TX_CTL,SDMMC_CMD,I2C1_SCL
35 A10SH_GPIO1	N20	IO, DQ3L, GPIO1_IO14,NAND_CE_N,UART1_TX,EMAC2_RX_CLK,SDMMC_CCLK
23 TRACE_CIK	P20	IO, DQ3L, GPIO1_IO15,UART1_RX,TRACE_CLK,EMAC2_RX_CTL,SDMMC_DATA1
35 A10SH_GPIO2	K23	IO, DQ3L, GPIO1_IO16,NAND_ADQ8,UART1_CTS_N,QSPI_SS2,EMAC2_TXD0,SDMMC_DATA2
35 A10SH_GPIO3	L23	IO, DQ3L, GPIO1_IO17,NAND_ADQ9,UART1_RTS_N,QSPI_SS3,EMAC2_TXD1,SDMMC_DATA3,SPIM0_SS1_N
42 USER_DIPSW_HPS2	N23	IO, DQSN3L, GPIO1_IO18,NAND_ADQ10,EMAC2_RXD0,SDMMC_DATA4,SPIM0_MISO,EMAC1_MDIO,I2C_EMAC1_SDA
42 USER_LED_HPS3	N22	IO, DQS3L, GPIO1_IO19,NAND_ADQ11,TRACE_CLK,EMAC2_RXD1,SDMMC_DATA5,SPIM0_SS0_N,EMAC1_MDC,I2C_EMAC1_SCL
23 TRACE_D0	K22	IO, DQ3L, GPIO1_IO20,NAND_ADQ12,TRACE_D0,EMAC2_TXD2,SDMMC_DATA6,SPIM0_CLK,SPIS1_CLK,I2C_EMAC2_SDA
23 TRACE_D1	L22	IO, DQ3L, GPIO1_IO21,NAND_ADQ13,TRACE_D1,EMAC2_TXD3,SDMMC_DATA7,SPIM0_MOSI,SPIS1_MOSI,I2C_EMAC2_SCL
23 TRACE_D2	M22	IO, DQ3L, GPIO1_IO22,NAND_ADQ14,TRACE_D2,EMAC2_RXD2,SPIM0_MISO,SPIS1_SS0_N,EMAC0_MDIO,I2C_EMAC0_SDA
23 TRACE_D3	M21	IO, DQ3L, GPIO1_IO23,NAND_ADQ15,TRACE_D3,EMAC2_RXD3,SPIM0_SS0_N,SPIS1_MISO,EMAC0_MDC,I2C_EMAC0_SCL

0 R661

IO BANK 2L, 3V0,2V5,1V8 BANK

A10SOC_1517

HOSTPROCESSOR_I2C

IO_1V8 36,37,68

R501 4.7K

R500 4.7K

IO_3V3 69

U55

FXMA2102UMX

7	B0	A0	2
6	B1	A1	3
		OE	5
8	VCCB	VCCA	1
		GND	4

A10_2L_SDA 35,45

A10_2L_SCL 35,45

A10I2CEN 35

C437 0.1uF

C436 0.1uF

1.00k R4077

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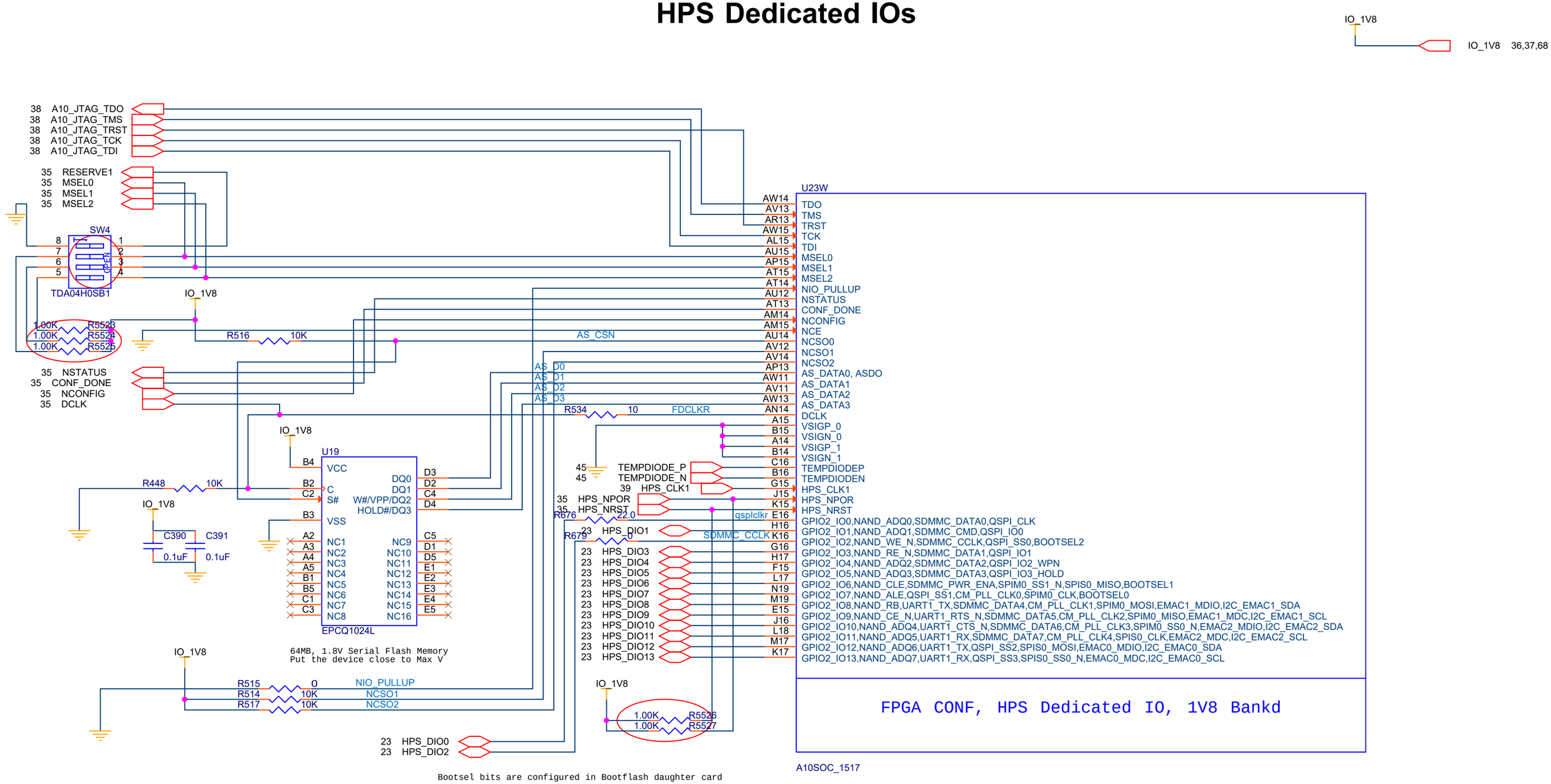
HPS Dedicated IOs



Bootsel bits are configured in Bootflash daughter card

Table 5-1: BOOTSEL Values for each Flash Memory Device Selection

BOOTSEL Field Value	Flash Device
0x0	Reserved
0x1	FPGA (HPS-to-FPGA bridge)
0x2	1.8V NAND flash memory
0x3	3.3V NAND flash memory
0x4	1.8V SD/MMC flash memory with external transceiver
0x5	3.3V SD/MMC flash memory with external transceiver
0x6	1.8V SPI or quad SPI flash memory
0x7	3.3V SPI or quad SPI flash memory

Table 7-3: MSEL Pin Settings for Each Configuration Scheme of Arria 10 Devices

Configuration Scheme	V_{CCPGM} (V)	Power-On Reset (POR) Delay	Valid MSEL[2..0]
FPP (x8, x16, and x32)	1.8	Fast	000
		Standard	001
PS	1.8	Fast	000
		Standard	001
AS (x1 and x4)	1.8	Fast	010
		Standard	011
JTAG-based configuration	—	—	Use any valid MSEL pin settings above

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10/100/1000 Ethernet - HPS

IO_1V8
R68 1.00K
R80 4.7K
R67 4.7K
R62 1.00K

20 ENET_HPS_MDC
20 ENET_HPS_MDIO
IO_3V3
35 ENET_HPS_RESETn
35 ENET_HPS_INTn

U12A
MDC 36
MDIO 37
RESET_N 42
INT_N/PME_N2 38

RX_CLK_PHYAD2 35
GTX_CLK 24
TX_EN 25
RX_DV_CLK125_EN 33
TXD3 22
TXD2 21
TXD1 20
TXD0 19
RXD0_MODE0 32
RXD1_MODE1 31
RXD2_MODE2 28
RXD3_MODE3 27
CLK125_NDO_LED_MODE 41

MDI_HPS_P0 2 TXRXP_A
MDI_HPS_N0 3 TXRXM_A
MDI_HPS_P1 5 TXRXP_B
MDI_HPS_N1 6 TXRXM_B
MDI_HPS_P2 7 TXRXP_C
MDI_HPS_N2 8 TXRXM_C
MDI_HPS_P3 10 TXRXP_D
MDI_HPS_N3 11 TXRXM_D
MDI INTERFACE

ISET 48
R340 12.1K
ENET_RSET

LED1_PHYAD0/PME_N1 17
LED2_PHYAD1 15
XI 46
XO 45

KSZ9031RN

IO_3V3
IO_5V
IO_2V5
IO_1V8
IO_3V3 69
IO_1V8 36,37,68
IO_2V5 36,68
IO_5V 50

ENET_HPS_RX_CLK 20
ENET_HPS_GTX_CLK 20
ENET_HPS_TX_EN 20
ENET_HPS_RX_DV 20
ENET_HPS_TXD3 20
ENET_HPS_TXD2 20
ENET_HPS_TXD1 20
ENET_HPS_TXD0 20
ENET_HPS_RXD0 20
ENET_HPS_RXD1 20
ENET_HPS_RXD2 20
ENET_HPS_RXD3 20

J5
YA 14 R7 220
YK 13 Yellow
TD0_P 11
CT0 12
TD0_N 10
TD1_P 4
CT1 6
TD1_N 5
TD2_P 3
CT2 1
TD2_N 2
TD3_P 8
CT3 7
TD3_N 9
GOA 16
GK 17 Green
OK 15 Orange
GND_TAB 18
GND_TAB 19
ENET_L829-1J1T-43

R8 220
IO_3V3

R5497 10K
U72 EN VCC GND OUT 25.00MHz
IO_2V5
C242 0.01uF

C15 0.01uF CT0
C13 0.01uF CT1
C12 0.01uF CT2
C14 0.01uF CT3

IO_1V8
R57 DNI ENET_HPS_LED2_LINK
R61 DNI ENET_HPS_LED1_LINK
R70 4.7K ENET_HPS_RXD3
R72 4.7K ENET_HPS_RXD2
R74 4.7K ENET_HPS_RXD1
R76 4.7K ENET_HPS_RXD0
R77 DNI ENET_HPS_RX_DV
R81 4.7K ENET_HPS_RX_CLK
R63 4.7K CLK125_NDO_LED_MODE
R367 4.7K
R378 4.7K
R69 DNI
R71 DNI
R73 DNI
R75 DNI
R78 4.7K
R79 DNI
R351 DNI
BOOT-STRAPS

U12B
1.2V_AVDLL_PLL
3.3V_AVDDH
1.8V_DVDDH
NC1 47
AVDDH 12
AVDDH 1
DVDDH 40
DVDDH 16
DVDDH 34
P_GND 49
NC 13
VSS 29
AVDDL_PLL 44
LDO_O 43
AVDDL 9
AVDDL 4
DVDDL 18
DVDDL 14
DVDDL 39
DVDDL 30
DVDDL 26
DVDDL 23
1.2V_AVDDL
1.2V_DVDDL
KSZ9031RN

IO_2V5
IO_5V
1.2V AVDLL_PLL
U10 LT3026-1
IN1 1
IN2 2
GNDS 4
SHDN 6
BST 5
OUT2 10
OUT1 9
ADJ 8
PG 7
GND 3
GND 11
C21 10uF
R342 10K
C26 1uF
R341 2.00K
R124 1.00K
C24 22uF
C22 2.2uF
1.2V_AVDLL_PLL

IO_3V3
C203 10uF
C37 10uF

IO_3V3
L15 3A, 30 Ohm FB
C210 22uF
C228 2.2uF
C230 0.1uF
3.3V_AVDDH
IO_1V8
L2 3A, 30 Ohm FB
C28 22uF
C262 2.2uF
C244 0.1uF
1.8V_DVDDH

1.2V_AVDLL_PLL
C16 22uF
C25 2.2uF
C261 0.1uF
L1 3A, 30 Ohm FB
C23 22uF
C243 2.2uF
C229 0.1uF
1.2V_AVDDL
L16 3A, 30 Ohm FB
C245 22uF
C280 2.2uF
C281 0.1uF
1.2V_DVDDL

Place near KSZ9021RN PHY

NAME	Pin	Value	Description
PHYAD2	35	1	ID = b"111"
PHYAD1	15	1	
PHYAD0	17	1	
MODE3	27	1	RGMII (10/100/1000)
MODE2	28	1	
MODE1	31	1	
MODE0	32	1	
ClK125_EN	33	0	No clockoutput
LED_MODE	41	1	singal led mode

ETHERNET INTERFACE

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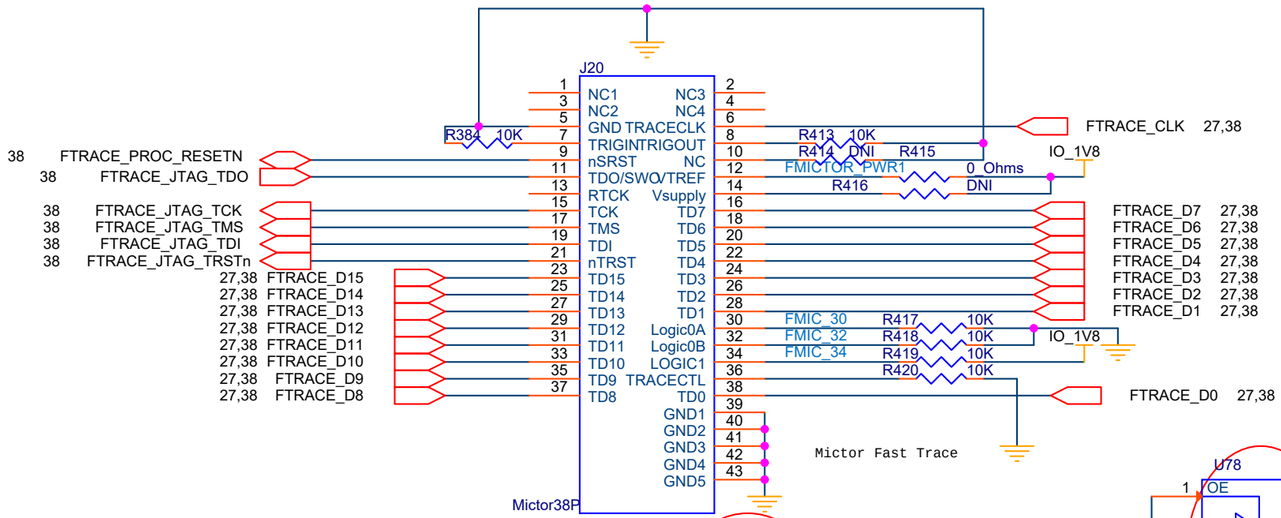
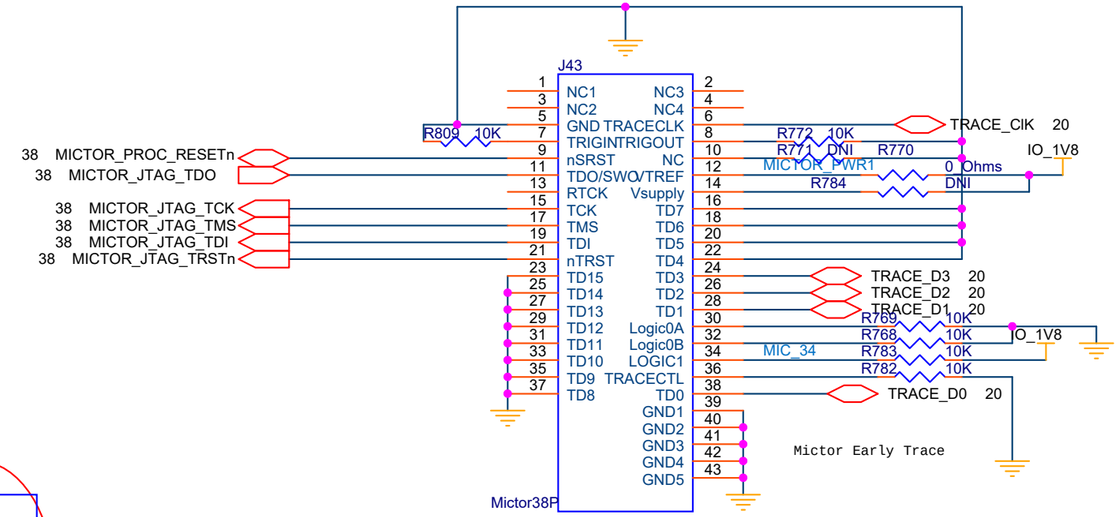
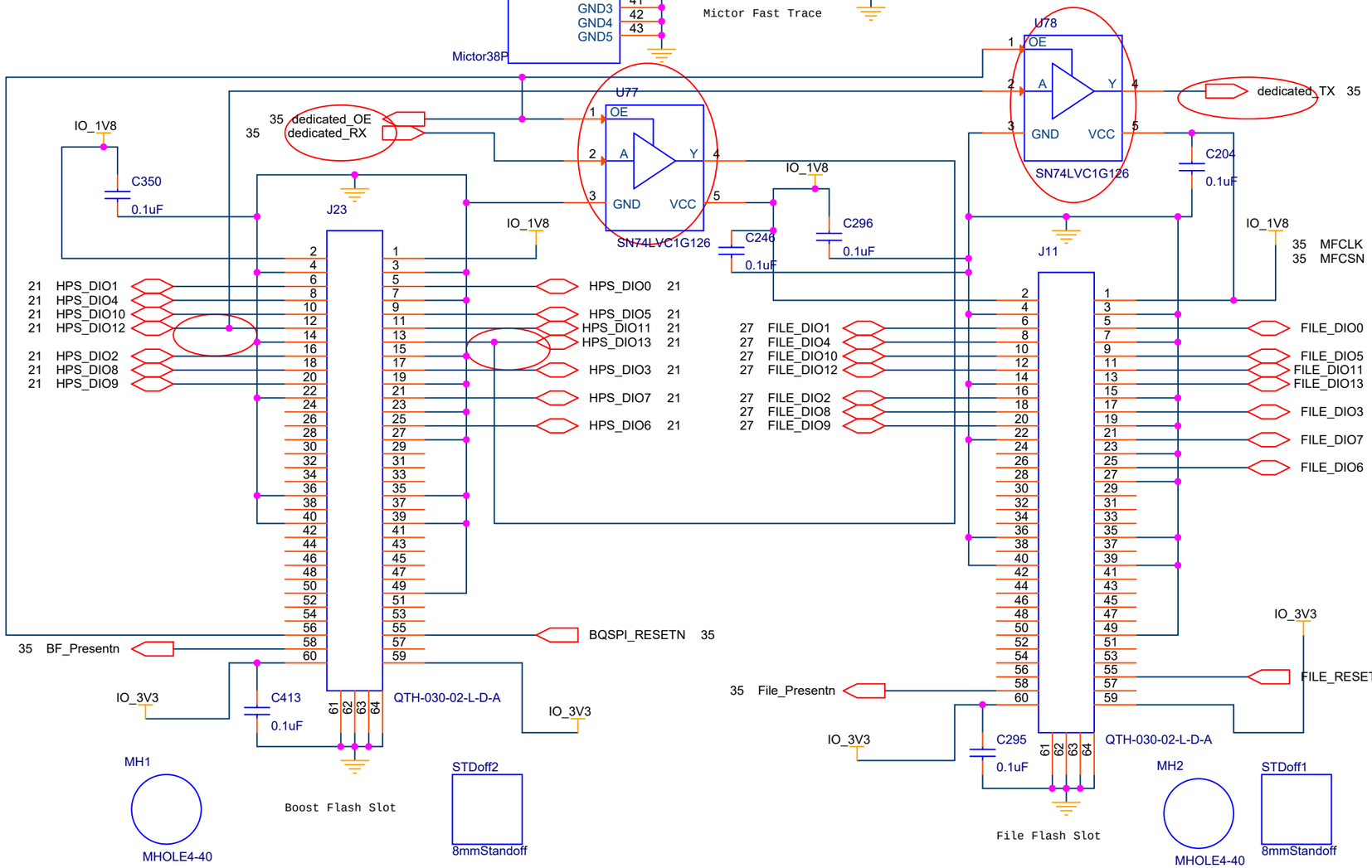
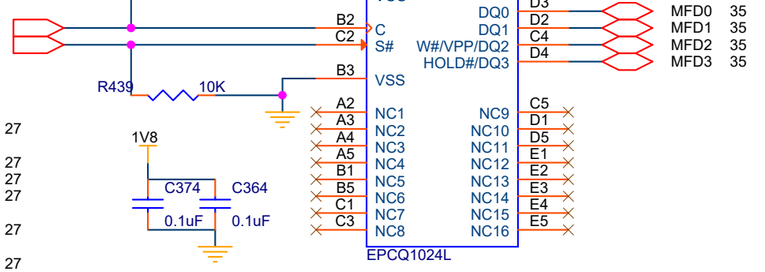
Connectors of Boot Flash, File Flash, Early Trace, and Fast Trace

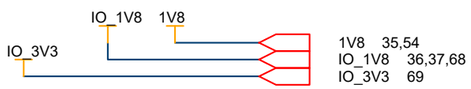








MAXV PS Flash



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External Memory Interface - HPS 40-bit 1GB HiLo Connector

J26A
HiLo EMI - EMI SIGNALS

19	HMEM_ADDR_CMD0	F1	MEM_ADDR_CMD0	MEM_DQ_ADDR_CMD0	R6
19	HMEM_ADDR_CMD1	H1	MEM_ADDR_CMD1	MEM_DQ_ADDR_CMD1	T1
19	HMEM_ADDR_CMD2	F2	MEM_ADDR_CMD2	MEM_DQ_ADDR_CMD2	R2
19	HMEM_ADDR_CMD3	G2	MEM_ADDR_CMD3	MEM_DQ_ADDR_CMD3	T2
19	HMEM_ADDR_CMD4	H2	MEM_ADDR_CMD4	MEM_DQ_ADDR_CMD4	U2
19	HMEM_ADDR_CMD5	J2	MEM_ADDR_CMD5	MEM_DQ_ADDR_CMD5	U3
19	HMEM_ADDR_CMD6	K2	MEM_ADDR_CMD6	MEM_DQ_ADDR_CMD6	T4
19	HMEM_ADDR_CMD7	G3	MEM_ADDR_CMD7	MEM_DQ_ADDR_CMD7	U4
19	HMEM_ADDR_CMD8	J3	MEM_ADDR_CMD8	MEM_DQ_ADDR_CMD8	T5
19	HMEM_ADDR_CMD9	L3	MEM_ADDR_CMD9		
19	HMEM_ADDR_CMD10	E4	MEM_ADDR_CMD10	MEM_DQS_ADDR_CMD_P	V4
19	HMEM_ADDR_CMD11	F4	MEM_ADDR_CMD11	MEM_DQS_ADDR_CMD_N	V5
19	HMEM_ADDR_CMD12	G4	MEM_ADDR_CMD12		
19	HMEM_ADDR_CMD13	H4	MEM_ADDR_CMD13		
19	HMEM_ADDR_CMD14	J4	MEM_ADDR_CMD14	MEM_CLK_P	V1
19	HMEM_ADDR_CMD15	K4	MEM_ADDR_CMD15	MEM_CLK_N	V2
19	HMEM_ADDR_CMD16	M1	MEM_ADDR_CMD16		
19	HMEM_ADDR_CMD17	M2	MEM_ADDR_CMD17		
19	HMEM_ADDR_CMD18	N2	MEM_ADDR_CMD18	CONFIG0	L6
19	HMEM_ADDR_CMD19	L4	MEM_ADDR_CMD19	CONFIG1	M6
19	HMEM_ADDR_CMD20	P5	MEM_ADDR_CMD20		
19	HMEM_ADDR_CMD21	M5	MEM_ADDR_CMD21		
19	HMEM_ADDR_CMD22	P1	MEM_ADDR_CMD22		
19	HMEM_ADDR_CMD23	R4	MEM_ADDR_CMD23		
19	HMEM_ADDR_CMD24	M4	MEM_ADDR_CMD24	RFU2	H5
19	HMEM_ADDR_CMD25	R3	MEM_ADDR_CMD25	RFU3	K5
19	HMEM_ADDR_CMD26	L2	MEM_ADDR_CMD26	RFU4	N6
19	HMEM_ADDR_CMD27	K1	MEM_ADDR_CMD27	RFU5	R7
19	HMEM_ADDR_CMD28	P2	MEM_ADDR_CMD28	RFU6	R8
19	HMEM_ADDR_CMD29	N4	MEM_ADDR_CMD29		
19	HMEM_ADDR_CMD30	P4	MEM_ADDR_CMD30		
19	HMEM_ADDR_CMD31	N3	MEM_ADDR_CMD31		

19	HPSMEM_DMA0	B10	MEM_DMA0	MEM_DMB0	M16
19	HPSMEM_DMA1	C4	MEM_DMA1	MEM_DMB1	U16
19	HPSMEM_DMA2	B17	MEM_DMA2	MEM_DMB2	U11
19	HPSMEM_DMA3	F17	MEM_DMA3	MEM_DMB3	U6
19	HMEM_DQA0	A4	MEM_DQA0	MEM_DQB0	H16
19	HMEM_DQA1	B4	MEM_DQA1	MEM_DQB1	J16
19	HMEM_DQA2	B5	MEM_DQA2	MEM_DQB2	K16
19	HMEM_DQA3	B6	MEM_DQA3	MEM_DQB3	L16
19	HMEM_DQA4	A8	MEM_DQA4	MEM_DQB4	H17
19	HMEM_DQA5	B8	MEM_DQA5	MEM_DQB5	K17
19	HMEM_DQA6	B9	MEM_DQA6	MEM_DQB6	K18
19	HMEM_DQA7	A10	MEM_DQA7	MEM_DQB7	L18
19	HMEM_DQA8	B1	MEM_DQA8	MEM_DQB8	M17
19	HMEM_DQA9	B2	MEM_DQA9	MEM_DQB9	N18
19	HMEM_DQA10	C2	MEM_DQA10	MEM_DQB10	P17
19	HMEM_DQA11	C3	MEM_DQA11	MEM_DQB11	P18
19	HMEM_DQA12	E3	MEM_DQA12	MEM_DQB12	R18
19	HMEM_DQA13	D4	MEM_DQA13	MEM_DQB13	T16
19	HMEM_DQA14	D1	MEM_DQA14	MEM_DQB14	T17
19	HMEM_DQA15	D2	MEM_DQA15	MEM_DQB15	T18
19	HMEM_DQA16	A12	MEM_DQA16	MEM_DQB16	U15
19	HMEM_DQA17	B12	MEM_DQA17	MEM_DQB17	T14
19	HMEM_DQA18	B13	MEM_DQA18	MEM_DQB18	U14
19	HMEM_DQA19	B14	MEM_DQA19	MEM_DQB19	V14
19	HMEM_DQA20	C15	MEM_DQA20	MEM_DQB20	T13
19	HMEM_DQA21	A16	MEM_DQA21	MEM_DQB21	T12
19	HMEM_DQA22	B16	MEM_DQA22	MEM_DQB22	U12
19	HMEM_DQA23	A18	MEM_DQA23	MEM_DQB23	V12
19	HMEM_DQA24	C16	MEM_DQA24	MEM_DQB24	T10
19	HMEM_DQA25	D16	MEM_DQA25	MEM_DQB25	U10
19	HMEM_DQA26	E16	MEM_DQA26	MEM_DQB26	V10
19	HMEM_DQA27	F16	MEM_DQA27	MEM_DQB27	T9
19	HMEM_DQA28	D17	MEM_DQA28	MEM_DQB28	T8
19	HMEM_DQA29	C18	MEM_DQA29	MEM_DQB29	U8
19	HMEM_DQA30	D18	MEM_DQA30	MEM_DQB30	U7
19	HMEM_DQA31	E18	MEM_DQA31	MEM_DQB31	V6
		E2	MEM_DQA32	MEM_DQB32	R16
		G16	MEM_DQA33	MEM_DQB33	T6
19	HMEM_DQSA_P0	A6	MEM_DQSA_P0	MEM_DQSB_P0	H18
19	HMEM_DQSA_N0	A7	MEM_DQSA_N0	MEM_DQSB_N0	J18
19	HMEM_DQSA_P1	A2	MEM_DQSA_P1	MEM_DQSB_P1	U18
19	HMEM_DQSA_N1	A3	MEM_DQSA_N1	MEM_DQSB_N1	V18
19	HMEM_DQSA_P2	A14	MEM_DQSA_P2	MEM_DQSB_P2	V16
19	HMEM_DQSA_N2	A15	MEM_DQSA_N2	MEM_DQSB_N2	V17
19	HMEM_DQSA_P3	F18	MEM_DQSA_P3	MEM_DQSB_P3	V8
19	HMEM_DQSA_N3	G18	MEM_DQSA_N3	MEM_DQSB_N3	V9
		A11	MEM_QKA_N0	MEM_QKB_N0	M18
		B18	MEM_QKA_N1	MEM_QKB_N1	V13

HLS-180324-B-12

HMEM_DQSB_N0
HMEM_DQSB_N1
HMEM_DQSB_N2
HMEM_DQSB_N3

HILOHPS_VDD
HMEM_DQSB_P0 R5332 1.00k
HMEM_DQSB_P1 R5333 1.00k
HMEM_DQSB_P2 R5334 1.00k
HMEM_DQSB_P3 R5335 1.00k
R5336 1.00k
R5337 1.00k
R5339 1.00k
R5338 1.00k

J26B
HiLo EMI - POWER

HILOHPS_VDD
C7 C9 C11 C13 D6 D8 D10 D12 D14 E7 E9 E11 E13 F6 F8 F10 — VDD
VDD = 1.1(DEFAULT)
62 HILOHPS_VDD

VDDQ_1.1V_SET and VDDQ_1.8V_SET NOT USED
Only support DDR3 and DDR4

62 HILOHPS_1V2_SETn
G15 — VDD_1.2V_SET
62 HILOHPS_1V35_SETn
D5 — VDD_1.25V_SET
62 HILOHPS_1V5_SETn
E15 — VDD_1.30V_SET
J15 — VDD_1.35V_SET
L15 — VDD_1.5V_SET
N16 — VDD_1.8V_SET

HILOHPS_VDD
F12 F14 G7 G9 G11 G13 H6 H8 H10 H12 — VDDQ
VDDQ = 1.1(DEFAULT)
N15 — VDDQ_1.1V_SET
P16 — VDDQ_1.2V_SET
F5 — VDDQ_1.25V_SET
R15 — VDDQ_1.30V_SET
R14 — VDDQ_1.35V_SET
R12 — VDDQ_1.5V_SET
R11 — VDDQ_1.8V_SET

VEXT = 2.5V
L11 L13 M8 M10 M12 M14 N7 N9 N11 N13 P8 P10 P12 P14 — VEXT

IO_2V5
IO_2V5 36,68

2.5V/3.3V (VTT)
J7 J9 K6 K8 K10 K12 J11 L7 L9

IO_3V3
IO_3V3 69

VREF
H14 J13 K14

HILOHPS_VDD
R5492 240
R5493 240
C1558 0.1uF

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HILOHPS_VDD
C511 10uF 1uF C596 0.1uF C595
Place near HILO connector J14 VDD pins

HILOHPS_VDD
C512 10uF 1uF C562 0.1uF C563
Place near HILO connector J14 VDDQ pins

J26C
HiLo EMI - GND

GND
A1 A5 A9 A13 A17 B3 B7 B11 B15 C1 C5 C6 C8 C10 C12 C14 C17 D3 D7 D9 D11 D13 D15 E1 E5 E6 E8 E10 E12 E14 E17 F3 F7 F9 F11 F13 F15 G1 G5 G6 G8 G10 G12 G14 G17 H3 H7 H9 H11 H13 H15 J1 J5 J6 J8 — GND
J10 J12 J14 J17 K3 K7 K9 K11 K13 K15 L1 L5 L8 L10 L12 L14 L17 M3 M7 M9 M11 M13 M15 N1 N5 N8 N10 N12 N14 N17 P3 P6 P7 P9 P11 P13 P15 R1 R5 R9 R10 R13 R17 T3 T7 T11 T15 U1 U5 U9 U13 U17 V3 V7 V11 V15 — GND

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USB Ports

USB 2.0 OTG

USB INTERFACE

Current limit for Rseti of 137k is 1.013A

35 USB_VFlagn

20 USB_DATA0
20 USB_DATA1
20 USB_DATA2
20 USB_DATA3
20 USB_DATA4
20 USB_DATA5
20 USB_DATA6
20 USB_DATA7

IO_5V
C10 2.2uF
U4 MAX14523B
IN NC1 NC2 FLAG ON OUT SETI GND GND_PAD
USB_5.0V
R17 137K 1%
C4 0.1uF
USB_VFlagn
R45 DNI
R302 10K

IO_1V8
IO_3V3
USB_1V8
reg_out
C483 4.7uF

U22 USB3320
DATA0 DATA1 DATA2 DATA3 DATA4 DATA5 DATA6 DATA7
VDDIO VDD3.3 VBAT VDD1.8 VDD1.8 NC
CPEN SPK_r SPK_l VBUS DM DP ID XO REFCLK REFSEL2 REFSEL0 REFSEL1 GND_FLAG
CLKOUT NXT DIR STP RBIAS RESET

USB_CPEN
USB_VBUS
USB_D_N
USB_D_P
USB_ID
USB_XO
USB_XI
IO_1V8
Y4 24MHz
C62 30pF
C61 30pF
R106 1M

10K
R560 R561 R562 R563 R564 R565 R566 R567
USB_DATA0 USB_DATA1 USB_DATA2 USB_DATA3 USB_DATA4 USB_DATA5 USB_DATA6 USB_DATA7
IO_3V3
R513 DNI

USB_CLKR USB_NXTR USB_DIRR USB_STP USB_RBIAS USB_RESET_PHY
R101 8.06K
R99 1.00K

20 USB_CLK
20 USB_NXT
20 USB_DIR
20 USB_STP
R105 10
R102 10
R104 10

35 USB_RESET
R98 1.00K USB_RESET_PHY

USB_5.0V
C5 4.7uF
J4 MICRO_USB_CONN
VBUS D- D+ ID
R100 1.00K

REFSEL[2:0] = 0X7, Reference Frequency = 24Mhz

IO_3V3
IO_3V3 69
IO_5V
IO_5V 50
USB_1V8
R103 0
IO_1V8
IO_1V8 36,37,68

USB_FPGA_5.0V
C889 1uF
U32 LT3010
IN NC7 NC6 SHDNn OUT SENSE NC3 GND EPAD
R767 2.21K
C153 0.01uF
C881 1uF
R227 5.23K

USB HPS Port

USB FPGA INTERFACE

USB TI GUI Port

36 USB_MAXV_D0
36 USB_MAXV_D1
36 USB_MAXV_D2
36 USB_MAXV_D3
36 USB_MAXV_D4
36 USB_MAXV_D5
36 USB_MAXV_D6
36 USB_MAXV_D7

USB_FPGA_1.8V
USB_FPGA_3.3V
USB_FPGA_5.0V

U33 FT245RQ
DATA0 DATA1 DATA2 DATA3 DATA4 DATA5 DATA6 DATA7
VCCIO VCC 3V3VOUT
USBDM USBDP TXE# RXF# OSCI OSCO PWREN# RESET# TEST
GND GND GND AGND GND_PAD
NC0 NC1 NC2 NC3 NC4 NC5

10K
R245 R262 R259 R267 R246 R264 R265 R263

36USB_MAXV_WR
36USB_MAXV_RDn
36USB_MAXV_RESET
R766 0
USB_F_RESET_PHY
R228 4.7K
USB_FPGA_1.8V

C168 4.7uF
5V_F_USB C171 0.01uF
J47 MICRO_USB_CONN
3A, 30 Ohm FB L14
USB_F_D_N
USB_F_D_P
R266 0
USB_FPGA_2.5V
R268 10K

USB_MAXV_TXEn 36
USB_MAXV_RXFn 36

PLACE NEAR USB3320

USB_1V8
C485 0.1uF
C460 0.1uF
C459 0.1uF
C472 0.1uF
IO_1V8
C473 0.1uF
IO_3V3
C458 4.7uF
C471 0.1uF
C484 0.1uF

MAX USB

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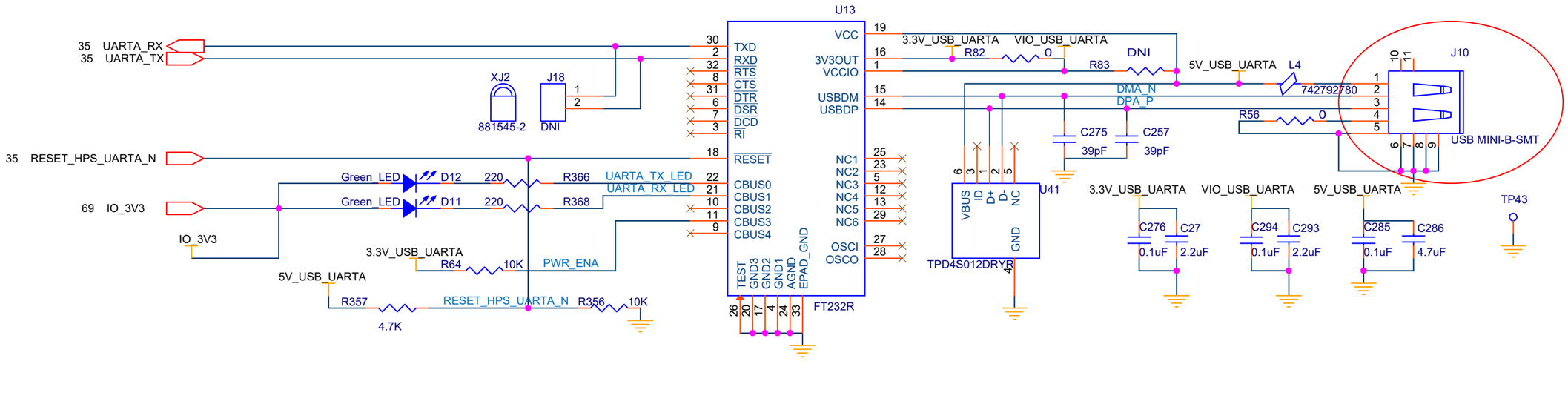
UART to USB PORT

UART



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Solutions

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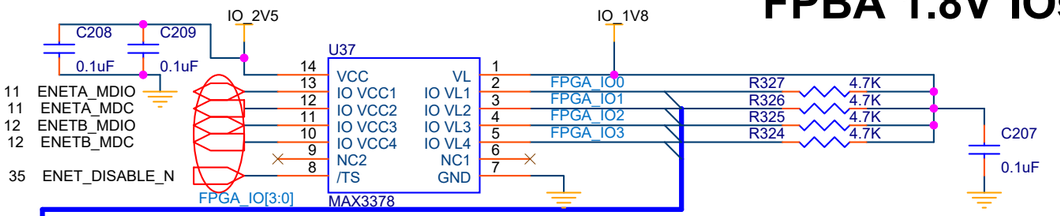
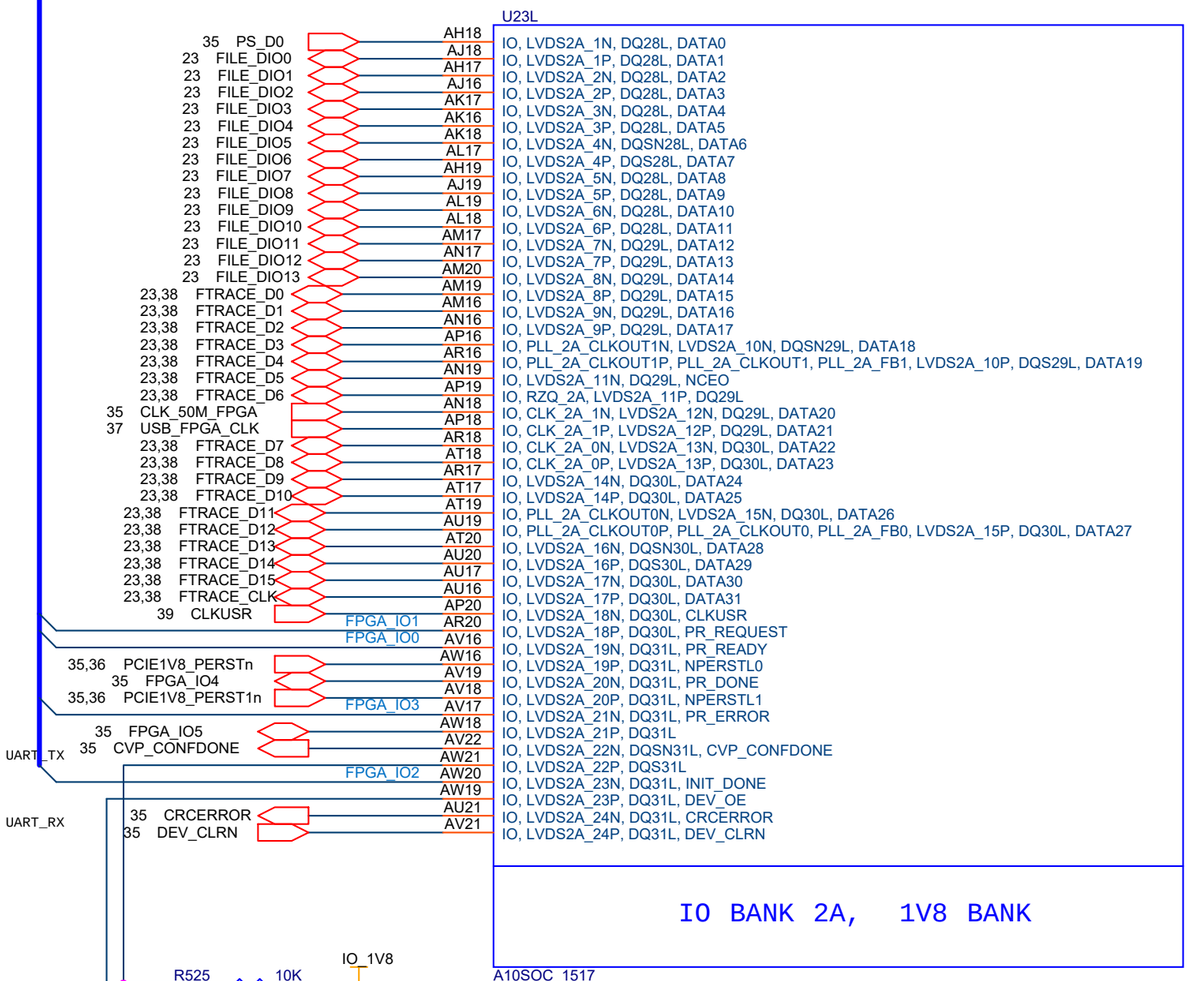
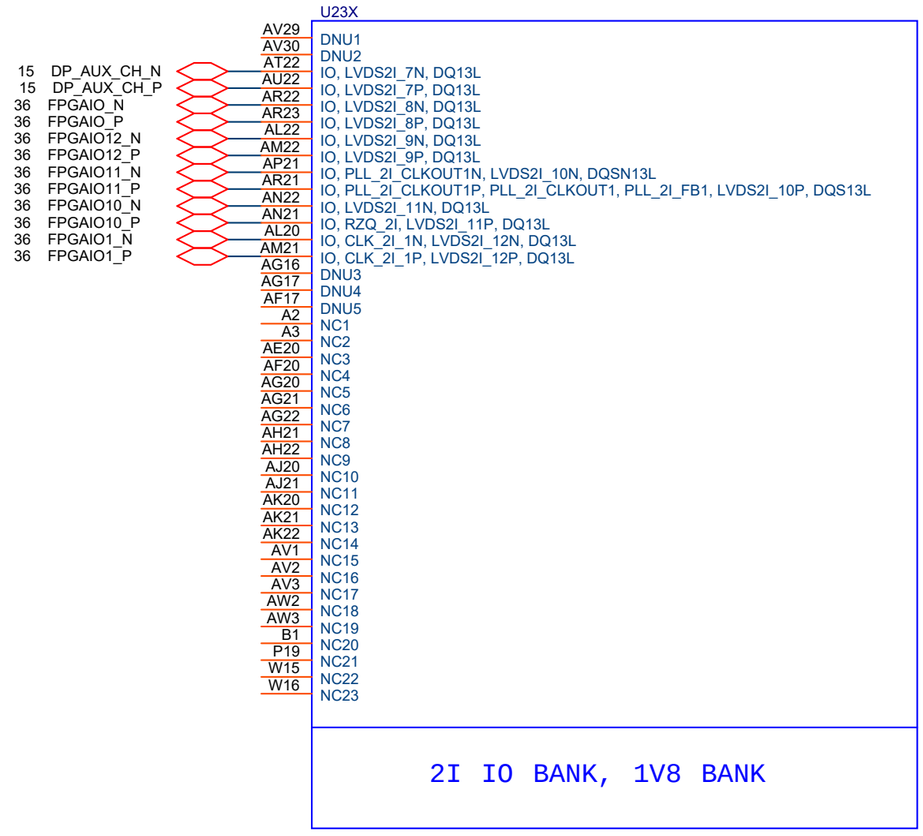
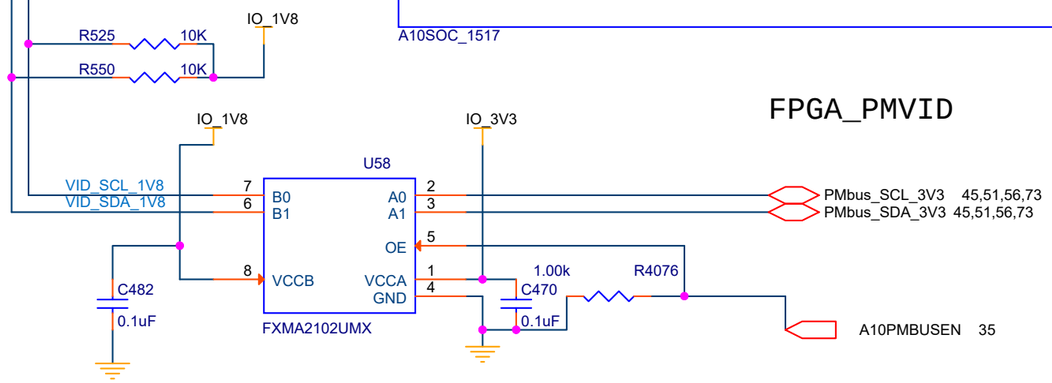
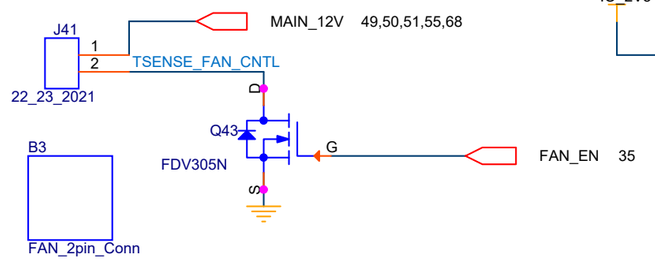
FPBA 1.8V IOs for File Flash and Debug Port

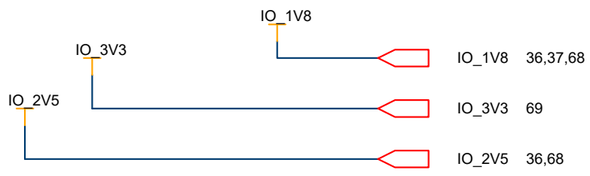












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FPGA IOs for LVDS Links of FMC A Port

U23M

17	FAHAN0	P15	IO, LVDS3H_1N, DQ32R
17	FAHAP0	P14	IO, LVDS3H_1P, DQ32R
17	FAHAN1	N14	IO, LVDS3H_2N, DQ32R
17	FAHAP1	M14	IO, LVDS3H_2P, DQ32R
17	FAHAN2	J14	IO, LVDS3H_3N, DQ32R
17	FAHAP2	J13	IO, LVDS3H_3P, DQ32R
17	FAHAN3	L15	IO, LVDS3H_4N, DQSN32R
17	FAHAP3	L14	IO, LVDS3H_4P, DQS32R
17	FAHAN4	L13	IO, LVDS3H_5N, DQ32R
17	FAHAP4	L12	IO, LVDS3H_5P, DQ32R
17	FAHAN5	K13	IO, LVDS3H_6N, DQ32R
17	FAHAP5	K12	IO, LVDS3H_6P, DQ32R
17	FALAN0	H14	IO, LVDS3H_7N, DQ33R
17	FALAP0	G14	IO, LVDS3H_7P, DQ33R
17	FALAN3	D14	IO, LVDS3H_8N, DQ33R
17	FALAP3	C14	IO, LVDS3H_8P, DQ33R
17	FALAN2	D13	IO, LVDS3H_9N, DQ33R
17	FALAP2	C13	IO, LVDS3H_9P, DQ33R
43	FA_LA_DEVCLK_N	E13	IO, PLL_3H_CLKOUT1N, LVDS3H_10N, DQSN33R
43	FA_LA_DEVCLK_P	E12	IO, PLL_3H_CLKOUT1P, PLL_3H_CLKOUT1, PLL_3H_FB1, LVDS3H_10P, DQS33R
17	FALAN4	H13	IO, LVDS3H_11N, DQ33R
		H12	IO, RZQ_3H, LVDS3H_11P, DQ33R
43	FA_LA_SYSREF_N	F14	IO, CLK_3H_1N, LVDS3H_12N, DQ33R
43	FA_LA_SYSREF_P	F13	IO, CLK_3H_1P, LVDS3H_12P, DQ33R
17	FAHAN6	C12	IO, CLK_3H_0N, LVDS3H_13N, DQ34R
17	FAHAP6	C11	IO, CLK_3H_0P, LVDS3H_13P, DQ34R
17	FAHAN7	E11	IO, LVDS3H_14N, DQ34R
17	FAHAP7	D11	IO, LVDS3H_14P, DQ34R
17	FAHAN8	G12	IO, PLL_3H_CLKOUT0N, LVDS3H_15N, DQ34R
17	FAHAP8	F12	IO, PLL_3H_CLKOUT0P, PLL_3H_CLKOUT0, PLL_3H_FB0, LVDS3H_15P, DQ34R
17	FAHAN9	G10	IO, LVDS3H_16N, DQSN34R
17	FAHAP9	F10	IO, LVDS3H_16P, DQS34R
17	FAHAN10	E10	IO, LVDS3H_17N, DQ34R
17	FAHAP10	D10	IO, LVDS3H_17P, DQ34R
17	FAHAN11	H11	IO, LVDS3H_18N, DQ34R
17	FAHAP11	G11	IO, LVDS3H_18P, DQ34R
17	FALAN6	B10	IO, LVDS3H_19N, DQ35R
17	FALAP6	A10	IO, LVDS3H_19P, DQ35R
17	FALAN7	B9	IO, LVDS3H_20N, DQ35R
17	FALAP7	A9	IO, LVDS3H_20P, DQ35R
17	FALAN8	B12	IO, LVDS3H_21N, DQ35R
17	FALAP8	B11	IO, LVDS3H_21P, DQ35R
17	FALAN9	A13	IO, LVDS3H_22N, DQSN35R
17	FALAP9	A12	IO, LVDS3H_22P, DQS35R
17	FALAN10	A8	IO, LVDS3H_23N, DQ35R
17	FALAP10	A7	IO, LVDS3H_23P, DQ35R
17	FALAN11	D9	IO, LVDS3H_24N, DQ35R
17	FALAP11	C9	IO, LVDS3H_24P, DQ35R

IO BANK 3H, 1V8 BANK

A10SOC_1517

17 FALAP4 — 0 — R671 — RZQ_3H

R659 DNI

17 FALAP16 — 0 — R670 — RZQ_3G

R658 DNI

43 FPGA_RCLK_3Gn

43 FPGA_RCLK_3Gp

43 FA_EMI_CLKN — R653 100 — 43 FA_EMI_CLKP

U23N

17	FAHAN12	F8	IO, LVDS3G_1N, DQ36R
17	FAHAP12	E8	IO, LVDS3G_1P, DQ36R
17	FAHAN13	C7	IO, LVDS3G_2N, DQ36R
17	FAHAP13	B7	IO, LVDS3G_2P, DQ36R
17	FAHAN14	D8	IO, LVDS3G_3N, DQ36R
17	FAHAP14	C8	IO, LVDS3G_3P, DQ36R
17	FAHAN15	C6	IO, LVDS3G_4N, DQSN36R
17	FAHAP15	B6	IO, LVDS3G_4P, DQS36R
17	FAHAN16	B5	IO, LVDS3G_5N, DQ36R
17	FAHAP16	A5	IO, LVDS3G_5P, DQ36R
17	FAHAN17	B4	IO, LVDS3G_6N, DQ36R
17	FAHAP17	A4	IO, LVDS3G_6P, DQ36R
17	FALAN20	C4	IO, LVDS3G_7N, DQ37R
17	FALAP20	C3	IO, LVDS3G_7P, DQ37R
17	FALAN21	D3	IO, LVDS3G_8N, DQ37R
17	FALAP21	C2	IO, LVDS3G_8P, DQ37R
17	FAHAN22	F7	IO, LVDS3G_9N, DQ37R
17	FAHAP22	E7	IO, LVDS3G_9P, DQ37R
17	FALAN15	D5	IO, PLL_3G_CLKOUT1N, LVDS3G_10N, DQSN37R
17	FALAP15	D4	IO, PLL_3G_CLKOUT1P, PLL_3G_CLKOUT1, PLL_3G_FB1, LVDS3G_10P, DQS37R
17	FALAN16	E6	IO, LVDS3G_11N, DQ37R
		D6	IO, RZQ_3G, LVDS3G_11P, DQ37R
		F5	IO, CLK_3G_1N, LVDS3G_12N, DQ37R
		E5	IO, CLK_3G_1P, LVDS3G_12P, DQ37R
17	FAHAN19	H9	IO, CLK_3G_0N, LVDS3G_13N, DQ38R
17	FAHAP19	H8	IO, CLK_3G_0P, LVDS3G_13P, DQ38R
17	FALAN17	G9	IO, LVDS3G_14N, DQ38R
17	FALAP17	F9	IO, LVDS3G_14P, DQ38R
		K8	IO, PLL_3G_CLKOUT0N, LVDS3G_15N, DQ38R
		J8	IO, PLL_3G_CLKOUT0P, PLL_3G_CLKOUT0, PLL_3G_FB0, LVDS3G_15P, DQ38R
		G6	IO, LVDS3G_16N, DQSN38R
17	FALAN19	G5	IO, LVDS3G_16P, DQS38R
17	FALAP19	H7	IO, LVDS3G_17N, DQ38R
17	FALAN18	G7	IO, LVDS3G_17P, DQ38R
17	FALAP18	J6	IO, LVDS3G_18N, DQ38R
17	FAHAN23	H6	IO, LVDS3G_18P, DQ38R
17	FAHAP23	L10	IO, LVDS3G_19N, DQ39R
17	FAHAN20	K10	IO, LVDS3G_19P, DQ39R
17	FAHAP20	K11	IO, LVDS3G_20N, DQ39R
17	FALAN13	J11	IO, LVDS3G_20P, DQ39R
17	FALAP13	N13	IO, LVDS3G_21N, DQ39R
17	FALAN12	M12	IO, LVDS3G_21P, DQ39R
17	FALAP12	N11	IO, LVDS3G_22N, DQSN39R
17	FAHAN21	M10	IO, LVDS3G_22P, DQS39R
17	FAHAP21	J10	IO, LVDS3G_23N, DQ39R
17	FALAN14	J9	IO, LVDS3G_23P, DQ39R
17	FALAP14	N12	IO, LVDS3G_24N, DQ39R
17	FAHAN18	M11	IO, LVDS3G_24P, DQ39R
17	FAHAP18		

IO BANK 3G, 1V8 BANK

A10SOC_1517

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FPGA IOs for LVDS Links of FMC A Port and FMC B Port

U23O

17	FALAN22	G4	IO, LVDS3F_1N, DQ40R
17	FALAP22	F4	IO, LVDS3F_1P, DQ40R
17	FALAN23	D1	IO, LVDS3F_2N, DQ40R
17	FALAP23	C1	IO, LVDS3F_2P, DQ40R
17	FALAN24	E2	IO, LVDS3F_3N, DQ40R
17	FALAP24	E1	IO, LVDS3F_3P, DQ40R
17	FALAN25	F3	IO, LVDS3F_4N, DQSN40R
17	FALAP25	E3	IO, LVDS3F_4P, DQS40R
17	FALAN26	G2	IO, LVDS3F_5N, DQ40R
17	FALAP26	F2	IO, LVDS3F_5P, DQ40R
17	FALAN27	H2	IO, LVDS3F_6N, DQ40R
17	FALAP27	G1	IO, LVDS3F_6P, DQ40R
17	FAHBN0	J5	IO, LVDS3F_7N, DQ41R
17	FAHBP0	J4	IO, LVDS3F_7P, DQ41R
17	FAHBN1	J1	IO, LVDS3F_8N, DQ41R
17	FAHBP1	H1	IO, LVDS3F_8P, DQ41R
17	FAHBN2	H4	IO, LVDS3F_9N, DQ41R
17	FAHBP2	H3	IO, LVDS3F_9P, DQ41R
17	FAHBN3	K2	IO, PLL_3F_CLKOUT1N, LVDS3F_10N, DQSN41R
17	FAHBP3	K1	IO, PLL_3F_CLKOUT1P, PLL_3F_CLKOUT1, PLL_3F_FB1, LVDS3F_10P, DQS41R
17	FAHBN4	L3	IO, LVDS3F_11N, DQ41R
		L2	IO, RZQ_3F, LVDS3F_11P, DQ41R
17	FAHBN5	K3	IO, CLK_3F_1N, LVDS3F_12N, DQ41R
17	FAHBP5	J3	IO, CLK_3F_1P, LVDS3F_12P, DQ41R
17	FAHBN6	N7	IO, CLK_3F_0N, LVDS3F_13N, DQ42R
17	FAHBP6	N6	IO, CLK_3F_0P, LVDS3F_13P, DQ42R
17	FAHBN7	K6	IO, LVDS3F_14N, DQ42R
17	FAHBP7	K5	IO, LVDS3F_14P, DQ42R
17	FAHBN8	L7	IO, PLL_3F_CLKOUT0N, LVDS3F_15N, DQ42R
17	FAHBP8	K7	IO, PLL_3F_CLKOUT0P, PLL_3F_CLKOUT0, PLL_3F_FB0, LVDS3F_15P, DQ42R
17	FAHBN9	M7	IO, LVDS3F_16N, DQSN42R
17	FAHBP9	M6	IO, LVDS3F_16P, DQS42R
17	FAHBN10	M4	IO, LVDS3F_17N, DQ42R
17	FAHBP10	L4	IO, LVDS3F_17P, DQ42R
17	FALAN28	M5	IO, LVDS3F_18N, DQ42R
17	FALAP28	L5	IO, LVDS3F_18P, DQ42R
17	FALAN29	P10	IO, LVDS3F_19N, DQ43R
17	FALAP29	N9	IO, LVDS3F_19P, DQ43R
17	FAHBN13	M9	IO, LVDS3F_20N, DQ43R
17	FAHBP13	N8	IO, LVDS3F_20P, DQ43R
17	FALAN30	R10	IO, LVDS3F_21N, DQ43R
17	FALAP30	P9	IO, LVDS3F_21P, DQ43R
17	FALAN31	R8	IO, LVDS3F_22N, DQSN43R
17	FALAP31	P8	IO, LVDS3F_22P, DQS43R
17	FALAN33	R11	IO, LVDS3F_23N, DQ43R
17	FALAP33	P11	IO, LVDS3F_23P, DQ43R
17	FALAN32	L9	IO, LVDS3F_24N, DQ43R
17	FALAP32	L8	IO, LVDS3F_24P, DQ43R

IO BANK 3F, 1V8 BANK

A10SOC_1517

U23P

36	FPGAIO9_N	M2	IO, LVDS3E_1N, DQ44R
36	FPGAIO9_P	M1	IO, LVDS3E_1P, DQ44R
36	FPGAIO8_N	N4	IO, LVDS3E_2N, DQ44R
36	FPGAIO8_P	N3	IO, LVDS3E_2P, DQ44R
36	FPGAIO7_N	R3	IO, LVDS3E_3N, DQ44R
36	FPGAIO7_P	R2	IO, LVDS3E_3P, DQ44R
36	FPGAIO6_N	N2	IO, LVDS3E_4N, DQSN44R
36	FPGAIO6_P	N1	IO, LVDS3E_4P, DQS44R
36	FPGAIO5_N	R1	IO, LVDS3E_5N, DQ44R
36	FPGAIO5_P	P1	IO, LVDS3E_5P, DQ44R
36	FPGAIO4_N	P4	IO, LVDS3E_6N, DQ44R
36	FPGAIO4_P	P3	IO, LVDS3E_6P, DQ44R
36	FPGAIO3_N	P6	IO, LVDS3E_7N, DQ45R
36	FPGAIO3_P	P5	IO, LVDS3E_7P, DQ45R
36	FPGAIO2_N	T5	IO, LVDS3E_8N, DQ45R
36	FPGAIO2_P	R5	IO, LVDS3E_8P, DQ45R
43	FBHA_N6	U7	IO, LVDS3E_9N, DQ45R
43	FBHA_P6	T7	IO, LVDS3E_9P, DQ45R
43	FPGA_Refsys_3En	U6	IO, PLL_3E_CLKOUT1N, LVDS3E_10N, DQSN45R
43	FPGA_Refsys_3Ep	U5	IO, PLL_3E_CLKOUT1P, PLL_3E_CLKOUT1, PLL_3E_FB1, LVDS3E_10P, DQS45R
43	FBHA_P17	V7	IO, LVDS3E_11N, DQ45R
		V6	IO, RZQ_3E, LVDS3E_11P, DQ45R
43	Refclk_3En	W6	IO, CLK_3E_1N, LVDS3E_12N, DQ45R
		W5	IO, CLK_3E_1P, LVDS3E_12P, DQ45R
18	FBLAN20	U4	IO, CLK_3E_0N, LVDS3E_13N, DQ46R
18	FBLAP20	T4	IO, CLK_3E_0P, LVDS3E_13P, DQ46R
18	FBLAN21	T3	IO, LVDS3E_14N, DQ46R
18	FBLAP21	T2	IO, LVDS3E_14P, DQ46R
18	FBLAN22	U2	IO, PLL_3E_CLKOUT0N, LVDS3E_15N, DQ46R
18	FBLAP22	U1	IO, PLL_3E_CLKOUT0P, PLL_3E_CLKOUT0, PLL_3E_FB0, LVDS3E_15P, DQ46R
18	FBLAN23	V2	IO, LVDS3E_16N, DQSN46R
18	FBLAP23	V1	IO, LVDS3E_16P, DQS46R
18	FBLAN24	W4	IO, LVDS3E_17N, DQ46R
18	FBLAP24	W3	IO, LVDS3E_17P, DQ46R
18	FBLAN25	V4	IO, LVDS3E_18N, DQ46R
18	FBLAP25	V3	IO, LVDS3E_18P, DQ46R
18	FBLAN26	U10	IO, LVDS3E_19N, DQ47R
18	FBLAP26	U9	IO, LVDS3E_19P, DQ47R
18	FBLAN27	V9	IO, LVDS3E_20N, DQ47R
18	FBLAP27	V8	IO, LVDS3E_20P, DQ47R
43	FBHA_N23	T9	IO, LVDS3E_21N, DQ47R
43	FBHA_P23	T8	IO, LVDS3E_21P, DQ47R
18	FBHA_N20	W10	IO, LVDS3E_22N, DQSN47R
18	FBHA_P20	W9	IO, LVDS3E_22P, DQS47R
43	FBHA_N21	V11	IO, LVDS3E_23N, DQ47R
43	FBHA_P21	U11	IO, LVDS3E_23P, DQ47R
18	FBHA_N22	R7	IO, LVDS3E_24N, DQ47R
18	FBHA_P22	R6	IO, LVDS3E_24P, DQ47R

IO BANK 3E, 1V8 BANK

A10SOC_1517

R609
100

RZQ_3E

17 FAHBP4 — 0 — R641 — RZQ_3F

R642
DNI

43 FBHA_N17 — 0 — R628

R629
DNI

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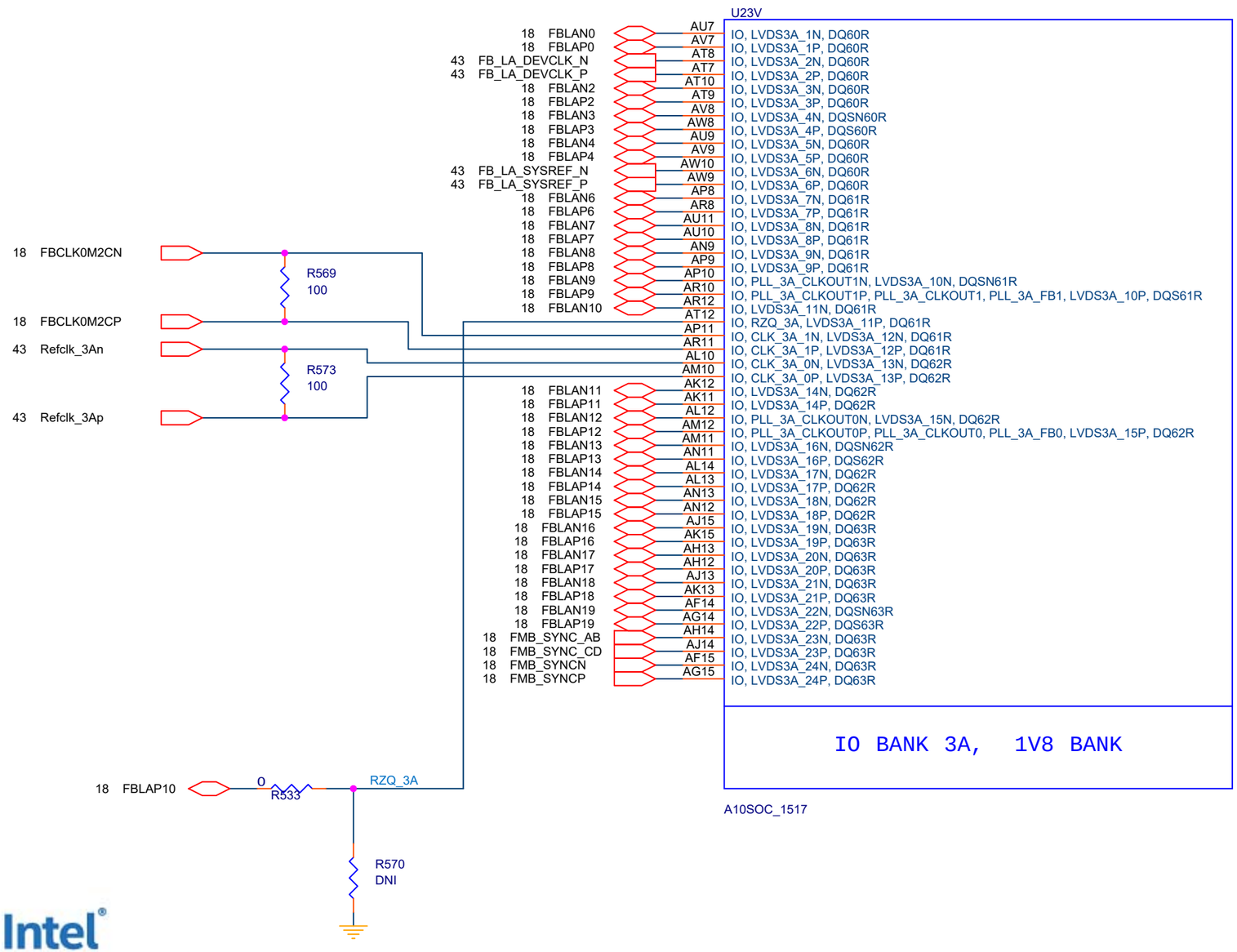
FPGA IOs for LVDS Links of FMC B Port



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FPGA IOs for FPGA Memory Interface

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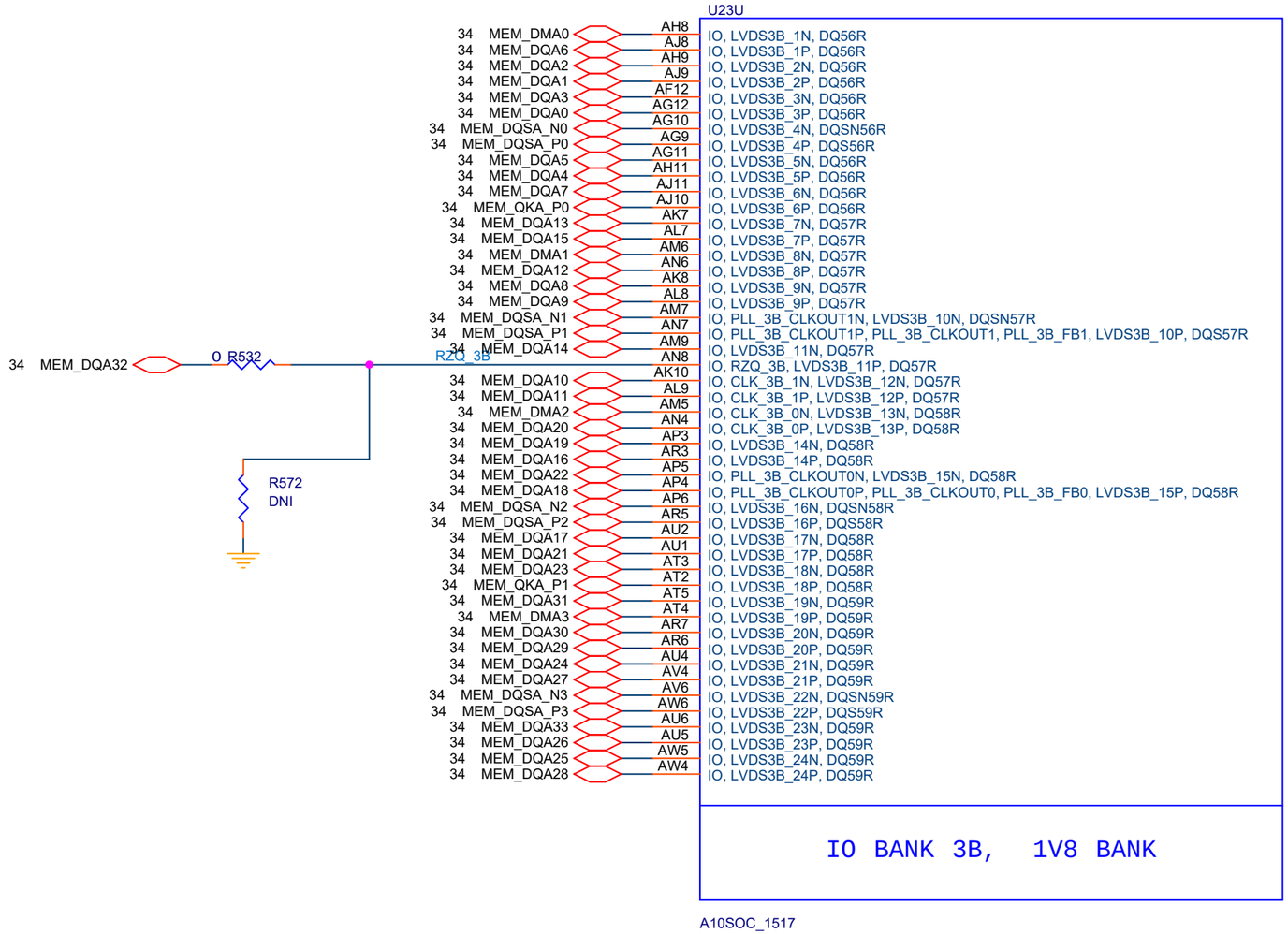
FPGA IOs for FPGA Memory Interface



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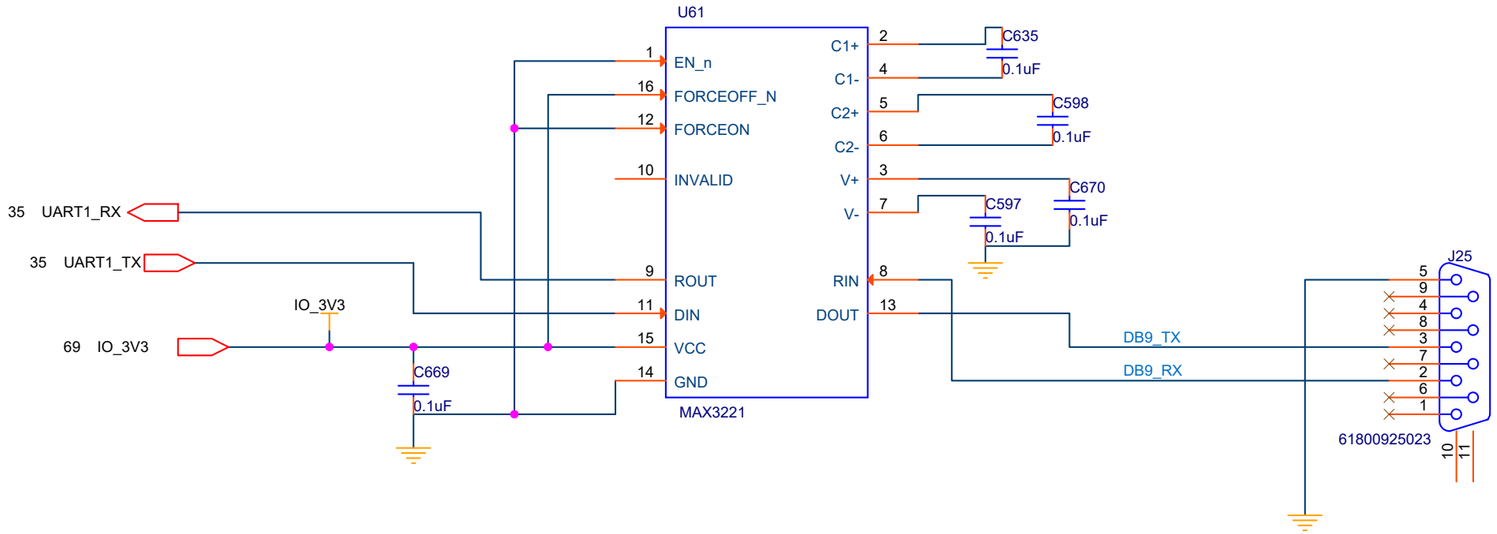
UART Port B



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External Memory Interface - HiLo Connector

J27A — HiLo EMI - EMI SIGNALS

31	MEM_ADDR_CMD0	F1	MEM_ADDR_CMD0	MEM_DQ_ADDR_CMD0	R6	MEM_DQ_ADDR_CMD0	31
31	MEM_ADDR_CMD1	H1	MEM_ADDR_CMD1	MEM_DQ_ADDR_CMD1	T1	MEM_DQ_ADDR_CMD1	31
31	MEM_ADDR_CMD2	F2	MEM_ADDR_CMD2	MEM_DQ_ADDR_CMD2	R2	MEM_DQ_ADDR_CMD2	31
31	MEM_ADDR_CMD3	G2	MEM_ADDR_CMD3	MEM_DQ_ADDR_CMD3	T2	MEM_DQ_ADDR_CMD3	31
31	MEM_ADDR_CMD4	H2	MEM_ADDR_CMD4	MEM_DQ_ADDR_CMD4	U2	MEM_DQ_ADDR_CMD4	31
31	MEM_ADDR_CMD5	J2	MEM_ADDR_CMD5	MEM_DQ_ADDR_CMD5	U3	MEM_DQ_ADDR_CMD5	31
31	MEM_ADDR_CMD6	K2	MEM_ADDR_CMD6	MEM_DQ_ADDR_CMD6	T4	MEM_DQ_ADDR_CMD6	31
31	MEM_ADDR_CMD7	G3	MEM_ADDR_CMD7	MEM_DQ_ADDR_CMD7	U4	MEM_DQ_ADDR_CMD7	31
31	MEM_ADDR_CMD8	J3	MEM_ADDR_CMD8	MEM_DQ_ADDR_CMD8	T5	MEM_DQ_ADDR_CMD8	31
31	MEM_ADDR_CMD9	L3	MEM_ADDR_CMD9				
31	MEM_ADDR_CMD10	E4	MEM_ADDR_CMD10	MEM_DQS_ADDR_CMD_P	V4	MEM_DQS_ADDR_CMD_P	31
31	MEM_ADDR_CMD11	F4	MEM_ADDR_CMD11	MEM_DQS_ADDR_CMD_N	V5	MEM_DQS_ADDR_CMD_N	31
31	MEM_ADDR_CMD12	G4	MEM_ADDR_CMD12				
31	MEM_ADDR_CMD13	H4	MEM_ADDR_CMD13	MEM_CLK_P	V1	MEM_CLK_P	31
31	MEM_ADDR_CMD14	J4	MEM_ADDR_CMD14	MEM_CLK_N	V2	MEM_CLK_N	31
31	MEM_ADDR_CMD15	K4	MEM_ADDR_CMD15				
31	MEM_ADDR_CMD16	M1	MEM_ADDR_CMD16				
31	MEM_ADDR_CMD17	M2	MEM_ADDR_CMD17	CONFIG0	L6		
31	MEM_ADDR_CMD18	N2	MEM_ADDR_CMD18	CONFIG1	M6		
31	MEM_ADDR_CMD19	L4	MEM_ADDR_CMD19				
31	MEM_ADDR_CMD20	P5	MEM_ADDR_CMD20				
31	MEM_ADDR_CMD21	M5	MEM_ADDR_CMD21				
31	MEM_ADDR_CMD22	P1	MEM_ADDR_CMD22				
31	MEM_ADDR_CMD23	R4	MEM_ADDR_CMD23				
31	MEM_ADDR_CMD24	M4	MEM_ADDR_CMD24	RFU2	H5		
31	MEM_ADDR_CMD25	R3	MEM_ADDR_CMD25	RFU3	K5		
31	MEM_ADDR_CMD26	L2	MEM_ADDR_CMD26	RFU4	N6		
31	MEM_ADDR_CMD27	K1	MEM_ADDR_CMD27	RFU5	R7		
31	MEM_ADDR_CMD28	P2	MEM_ADDR_CMD28	RFU6	R8		
31	MEM_ADDR_CMD29	N4	MEM_ADDR_CMD29				
31	MEM_ADDR_CMD30	P4	MEM_ADDR_CMD30				
31	MEM_ADDR_CMD31	N3	MEM_ADDR_CMD31				
32	MEM_DMA0	B10	MEM_DMA0	MEM_DMB0	M16	MEM_DMB0	31
32	MEM_DMA1	C4	MEM_DMA1	MEM_DMB1	U16	MEM_DMB1	31
32	MEM_DMA2	B17	MEM_DMA2	MEM_DMB2	U11	MEM_DMB2	31
32	MEM_DMA3	F17	MEM_DMA3	MEM_DMB3	U6	MEM_DMB3	31
32	MEM_DQA0	A4	MEM_DQA0	MEM_DQB0	H16	MEM_DQB0	31
32	MEM_DQA1	B4	MEM_DQA1	MEM_DQB1	J16	MEM_DQB1	31
32	MEM_DQA2	B5	MEM_DQA2	MEM_DQB2	K16	MEM_DQB2	3164
32	MEM_DQA3	B6	MEM_DQA3	MEM_DQB3	L16	MEM_DQB3	3164
32	MEM_DQA4	A8	MEM_DQA4	MEM_DQB4	H17	MEM_DQB4	3164
32	MEM_DQA5	B8	MEM_DQA5	MEM_DQB5	K17	MEM_DQB5	3164
32	MEM_DQA6	B9	MEM_DQA6	MEM_DQB6	K18	MEM_DQB6	3164
32	MEM_DQA7	A10	MEM_DQA7	MEM_DQB7	L18	MEM_DQB7	3164
32	MEM_DQA8	B1	MEM_DQA8	MEM_DQB8	M17	MEM_DQB8	31
32	MEM_DQA9	B2	MEM_DQA9	MEM_DQB9	N18	MEM_DQB9	31
32	MEM_DQA10	C2	MEM_DQA10	MEM_DQB10	P17	MEM_DQB10	31
32	MEM_DQA11	C3	MEM_DQA11	MEM_DQB11	P18	MEM_DQB11	31
32	MEM_DQA12	E3	MEM_DQA12	MEM_DQB12	R18	MEM_DQB12	31
32	MEM_DQA13	D4	MEM_DQA13	MEM_DQB13	T16	MEM_DQB13	31
32	MEM_DQA14	D1	MEM_DQA14	MEM_DQB14	T17	MEM_DQB14	31
32	MEM_DQA15	D2	MEM_DQA15	MEM_DQB15	T18	MEM_DQB15	31
32	MEM_DQA16	A12	MEM_DQA16	MEM_DQB16	U15	MEM_DQB16	31
32	MEM_DQA17	B12	MEM_DQA17	MEM_DQB17	T14	MEM_DQB17	31
32	MEM_DQA18	B13	MEM_DQA18	MEM_DQB18	U14	MEM_DQB18	31
32	MEM_DQA19	B14	MEM_DQA19	MEM_DQB19	V14	MEM_DQB19	31
32	MEM_DQA20	C15	MEM_DQA20	MEM_DQB20	T13	MEM_DQB20	31
32	MEM_DQA21	A16	MEM_DQA21	MEM_DQB21	T12	MEM_DQB21	31
32	MEM_DQA22	B16	MEM_DQA22	MEM_DQB22	U12	MEM_DQB22	31
32	MEM_DQA23	A18	MEM_DQA23	MEM_DQB23	V12	MEM_DQB23	31
32	MEM_DQA24	C16	MEM_DQA24	MEM_DQB24	T10	MEM_DQB24	31
32	MEM_DQA25	D16	MEM_DQA25	MEM_DQB25	U10	MEM_DQB25	31
32	MEM_DQA26	E16	MEM_DQA26	MEM_DQB26	V10	MEM_DQB26	31
32	MEM_DQA27	F16	MEM_DQA27	MEM_DQB27	T9	MEM_DQB27	31
32	MEM_DQA28	D17	MEM_DQA28	MEM_DQB28	T8	MEM_DQB28	31
32	MEM_DQA29	C18	MEM_DQA29	MEM_DQB29	U8	MEM_DQB29	31
32	MEM_DQA30	D18	MEM_DQA30	MEM_DQB30	U7	MEM_DQB30	31
32	MEM_DQA31	E18	MEM_DQA31	MEM_DQB31	V6	MEM_DQB31	31
32	MEM_DQA32	E2	MEM_DQA32	MEM_DQB32	R16	MEM_DQB32	31
32	MEM_DQA33	G16	MEM_DQA33	MEM_DQB33	T6	MEM_DQB33	31
32	MEM_DQSA_P0	A6	MEM_DQSA_P0	MEM_DQSB_P0	H18	MEM_DQSB_P0	31
32	MEM_DQSA_N0	A7	MEM_DQSA_N0	MEM_DQSB_N0	J18	MEM_DQSB_N0	31
32	MEM_DQSA_P1	A2	MEM_DQSA_P1	MEM_DQSB_P1	U18	MEM_DQSB_P1	31
32	MEM_DQSA_N1	A3	MEM_DQSA_N1	MEM_DQSB_N1	V18	MEM_DQSB_N1	31
32	MEM_DQSA_P2	A14	MEM_DQSA_P2	MEM_DQSB_P2	V16	MEM_DQSB_P2	31
32	MEM_DQSA_N2	A15	MEM_DQSA_N2	MEM_DQSB_N2	V17	MEM_DQSB_N2	31
32	MEM_DQSA_P3	F18	MEM_DQSA_P3	MEM_DQSB_P3	V8	MEM_DQSB_P3	31
32	MEM_DQSA_N3	G18	MEM_DQSA_N3	MEM_DQSB_N3	V9	MEM_DQSB_N3	31
32	MEM_QKA_P0	A11	MEM_QKA_N0	MEM_QKB_N0	M18	MEM_QKB_P0	31
32	MEM_QKA_P1	B18	MEM_QKA_N1	MEM_QKB_N1	V13	MEM_QKB_P1	31

HLS-180324-B-12

J27B — HiLo EMI - POWER

63 HILO_VDD

C7	VDD	
C9	VDD	
C11	VDD	
C13	VDD	
D6	VDD	
D8	VDD	VDD = 1.1(DEFAULT)
D10	VDD	
D12	VDD	
D14	VDD	
E7	VDD	
E9	VDD	
E11	VDD	
E13	VDD	
F6	VDD	
F8	VDD	
F10	VDD	

VEXT = 2.5V

L11	VEXT
L13	VEXT
M8	VEXT
M10	VEXT
M12	VEXT
M14	VEXT
N7	VEXT
N9	VEXT
N11	VEXT
N13	VEXT
P8	VEXT
P10	VEXT
P12	VEXT
P14	VEXT

IO_2V5

63 HILO_1V2_SETn
63 HILO_1V25_SETn
63 HILO_1V30_SETn
63 HILO_1V35_SETn
63 HILO_1V5_SETn
63 HILO_1V8_SETn

G15	VDD_1.2V_SET
D5	VDD_1.25V_SET
E15	VDD_1.30V_SET
J15	VDD_1.35V_SET
L15	VDD_1.5V_SET
N16	VDD_1.8V_SET

64 HILO_VDDQ

F12	VDDQ	
F14	VDDQ	
G7	VDDQ	
G9	VDDQ	VDDQ = 1.1(DEFAULT)
G11	VDDQ)	
G13	VDDQ	
H6	VDDQ	
H8	VDDQ	
H10	VDDQ	
H12	VDDQ	

2.5V/3.3V (VTT)

J7	2.5V/3.3V (VTT)
J9	2.5V/3.3V (VTT)
K6	2.5V/3.3V (VTT)
K8	2.5V/3.3V (VTT)
K10	2.5V/3.3V (VTT)
K12	2.5V/3.3V (VTT)
J11	2.5V/3.3V (VTT)
L7	2.5V/3.3V (VTT)
L9	2.5V/3.3V (VTT)

IO_3V3

N15	VDDQ_1.1V_SET	
P16	VDDQ_1.2V_SET	
F5	VDDQ_1.25V_SET	
R15	VDDQ_1.30V_SET	
R14	VDDQ_1.35V_SET	
R12	VDDQ_1.5V_SET	
R11	VDDQ_1.8V_SET	

63 HILOQ_1V2_SETn
63 HILOQ_1V25_SETn
63 HILOQ_1V30_SETn
63 HILOQ_1V35_SETn
63 HILOQ_1V5_SETn
63 HILOQ_1V8_SETn

VREF

H14	VREF
J13	VREF
K14	VREF

HILO_VDDQ

R5495 240

R5494 240

C1557 0.1uF

HLS-180324-B-12

J27C — HiLo EMI - GND

IO_2V5 36,66

IO_3V3 39

A1	GND	J10
A5	GND	J12
A9	GND	J14
A13	GND	J17
A17	GND	K3
B3	GND	K7
B7	GND	K9
B11	GND	K11
B15	GND	K13
C1	GND	K15
C5	GND	L1
C6	GND	L5
C8	GND	L8
C10	GND	L10
C12	GND	L12
C14	GND	L14
C17	GND	L17
D3	GND	M3
D7	GND	M7
D9	GND	M9
D11	GND	M11
D13	GND	M13
D15	GND	M15
E1	GND	N1
E5	GND	N5
E6	GND	N8
E8	GND	N10
E10	GND	N12
E12	GND	N14
E14	GND	N17
E17	GND	P3
F3	GND	P6
F7	GND	P7
F9	GND	P9
F11	GND	P11
F13	GND	P13
F15	GND	P15
G1	GND	R1
G5	GND	R5
G6	GND	R9
G8	GND	R10
G10	GND	R13
G12	GND	R17
G14	GND	T3
G17	GND	T7
H3	GND	T11
H7	GND	T15
H9	GND	U1
H11	GND	U5
H13	GND	U9
H15	GND	U13
J1	GND	U17
J5	GND	V3
J6	GND	V7
J8	GND	V11
	GND	V15
	GND	

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HILO_VDD

C639 10uF — C532 1uF — C601 0.1uF

Place near HILO connector J14 VDD pins

HILO_VDDQ

C600 10uF — C531 1uF — C640 0.1uF

Place near HILO connector J14 VDDQ pins

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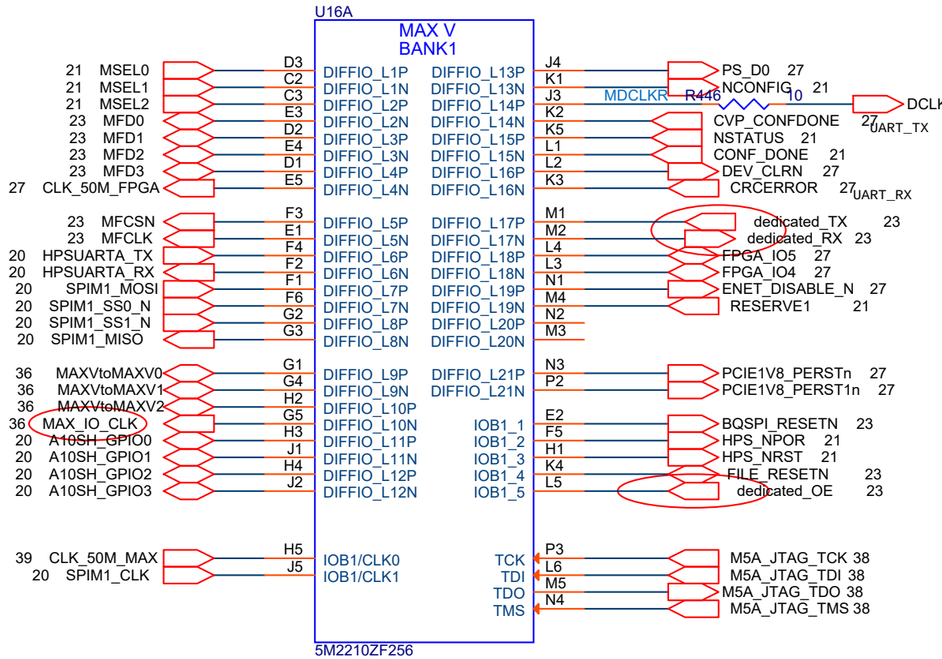
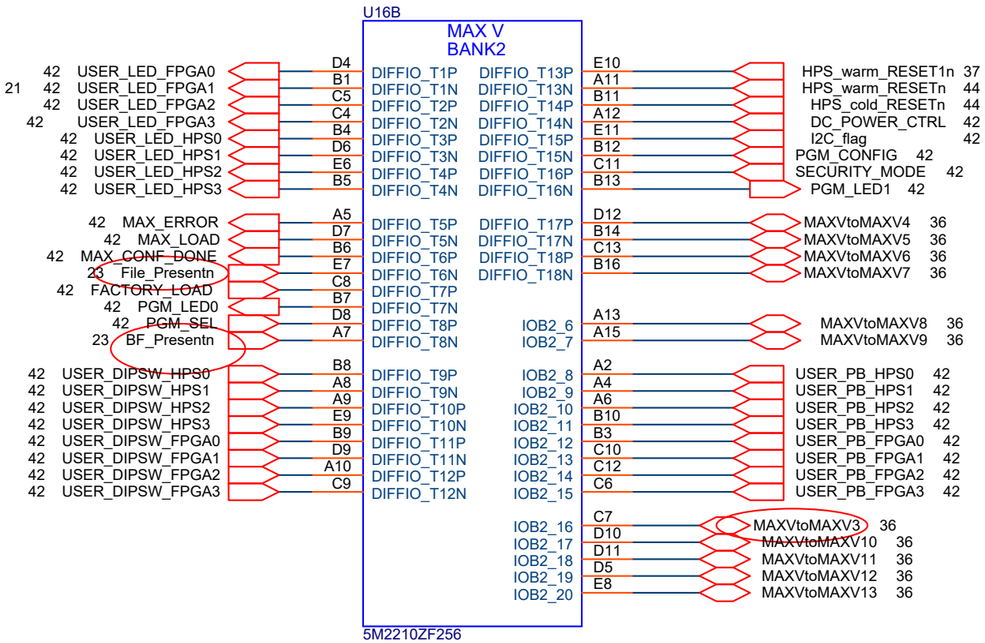
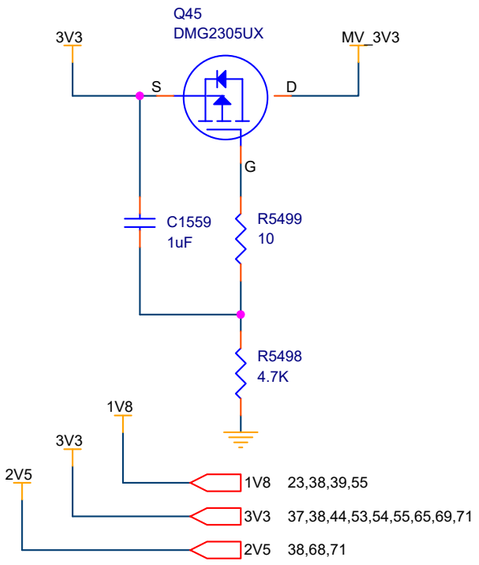
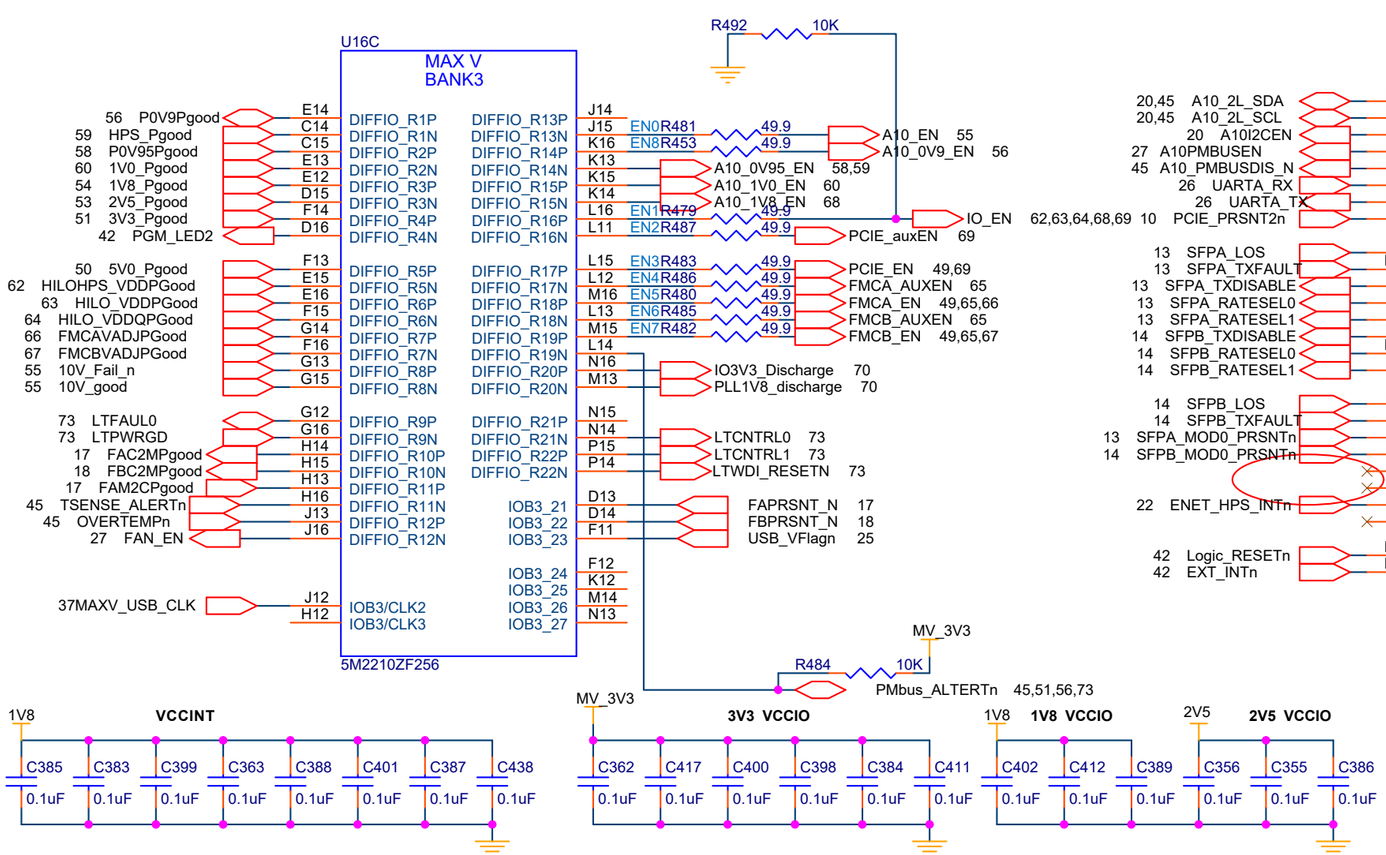
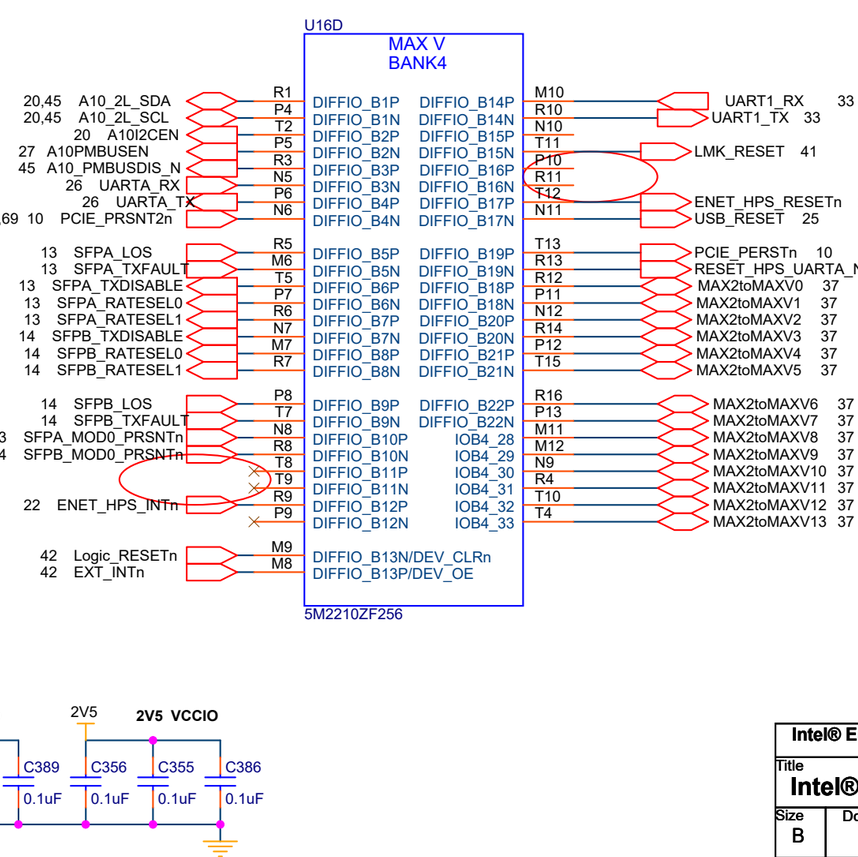
5M2210 System Controller

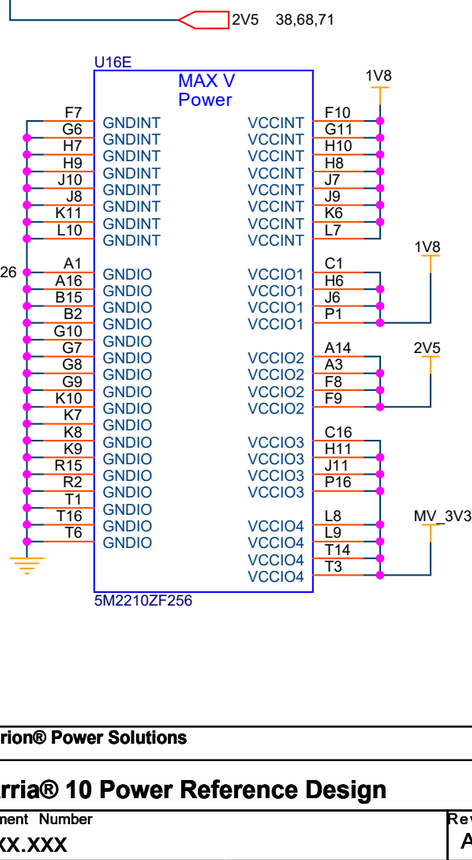












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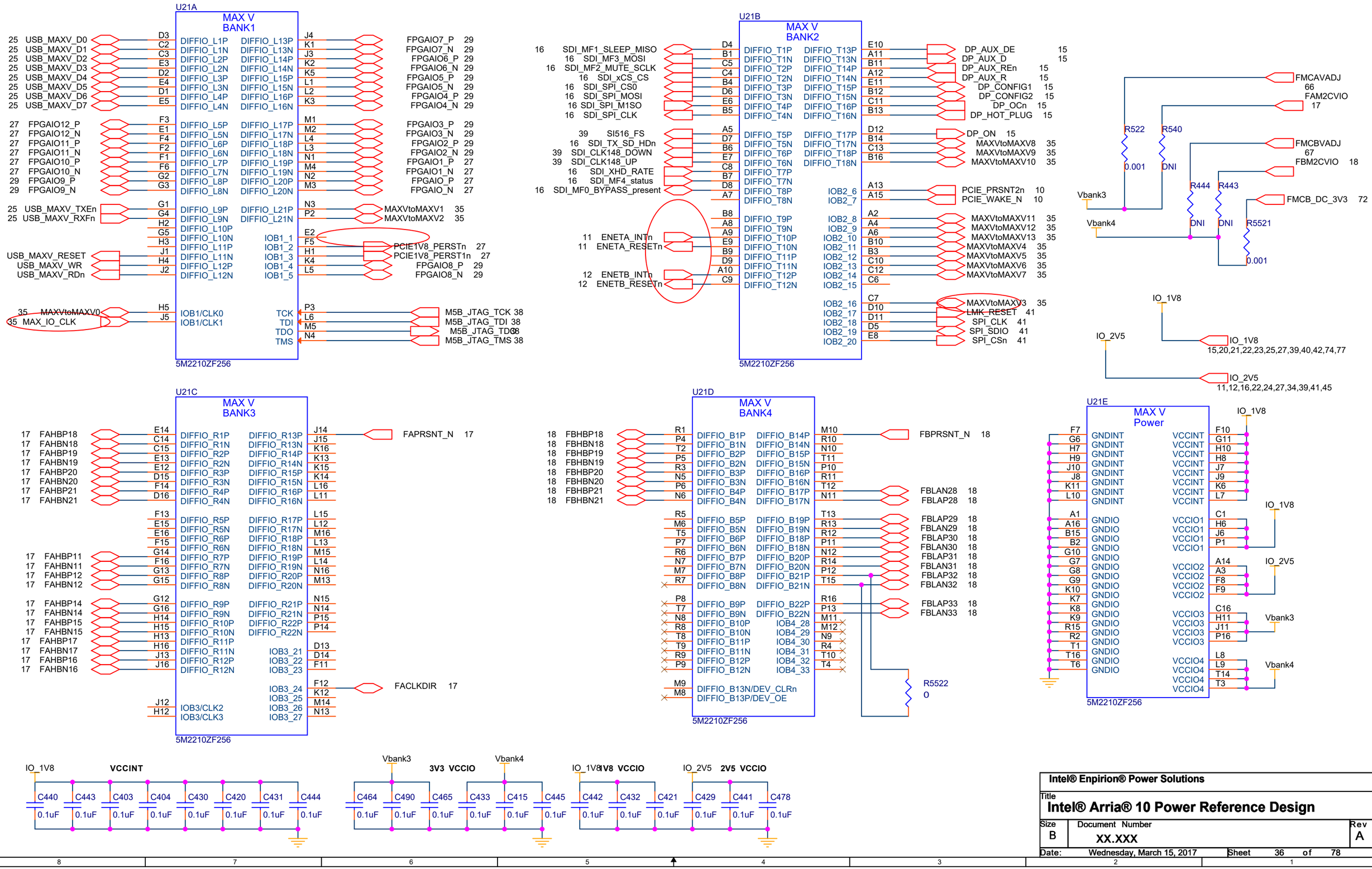
FPGAIO for DP_IO, SDI_IO and FMC_3V3IO



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On-Board USB Blaster II - Part 1

VBUS_5V R93 10K FX2_WAKEUP
R438 20K C57 0.1uF

J22 MICRO_USB_CONN
VBUS 1 VBUS_5V
D- 2 FX2_D_N
D+ 3 FX2_D_P
ID 4 R90 DNI
5
1M R412
4.7nF C347

U53 TPD2EUSB30
3 GND D+ 1 D- 2

C425 0.1uF
U20 MAX811
GND VCC
RESET MR
100K R97 FX2_RESETn
35 HPS_warm_RESET1n

3V3

U18 CY7C68013A_QFN
AVCC RESET 42
AVCC SCL 15 FX2_SCL R5459 2.00K
SDA 16 FX2_SDA R5460 2.00K
VCC WAKEUP 44 FX2_WAKEUP
VCC CTL0 29 FX2_FLAGA
VCC CTL1 30 FX2_FLAGB
VCC CTL2 31 FX2_FLAGC
VCC
VCC DMINUS 9
DPLUS 8
IFCLK 13 FX2_SLRDn
CLKOUT 54 FX2_SLWRn
XTALIN 5 24M_XTALIN
XTALOUT 4 24M_XTALOUT
IFCLK = 48MHz
PA0 33 FX2_PA0
PA1 34 FX2_PA1
PA2 35 FX2_PA2
PA3 36 FX2_PA3
PA4 37 FX2_PA4
PA5 38 FX2_PA5
PA6 39 FX2_PA6
PA7 40 FX2_PA7
PB0 18 FX2_PB0
PB1 19 FX2_PB1
PB2 20 FX2_PB2
PB3 21 FX2_PB3
PB4 22 FX2_PB4
PB5 23 FX2_PB5
PB6 24 FX2_PB6
PB7 25 FX2_PB7
RESERVED 14
AGND 6
AGND 10
GND 12
GND 26
GND 28
GND 41
GND 53
GND 56
PD0 45 FX2_PD0
PD1 46 FX2_PD1
PD2 47 FX2_PD2
PD3 48 FX2_PD3
PD4 49 FX2_PD4
PD5 50 FX2_PD5
PD6 51 FX2_PD6
PD7 52 FX2_PD7
GND EXPOSED_PAD 57

Y3 24.00MHz
C59 12pF
C60 12pF

FX2_PB[0:7]
FX2_PA[0:7]
FX2_PD[0:7]

U17A EPM1270_M256FBGA
MAX II BANK1
IOB1_1 B1 FX2_SCL
IOB1_2 C1 FX2_PB0
IOB1_3 C2
IOB1_4 C3
IOB1_5 C4
IOB1_6 D1 FX2_PB1
IOB1_7 D2
IOB1_8 D3
IOB1_9 D4
IOB1_10 E1 FX2_PB7
IOB1_11 E2
IOB1_12 E3
IOB1_13 E4
IOB1_14 F1 FX2_PB5
IOB1_15 F2
IOB1_16 F3
IOB1_17 F4
IOB1_18 G1 FX2_PB6
IOB1_19 G2 18 FBTDO
IOB1_20 G3
IOB1_21 G4
IOB1_22 H1 FX2_FLAGC
IOB1_23 H2 FX2_FLAGA
IOB1_24 H4
IOB1/GCLK0 K1 FX2_CLK FX2_PA0
IOB1/GCLK1 L1
IOB1_25 J1 FX2_FLAGB
IOB1_26 J2 PCIE_TRSTN 10
IOB1_27 K2 PCIE_TCK 10
IOB1_28 L2 PCIE_TMS 10
IOB1_29 M1 FX2_PA1
IOB1_30 M2
IOB1_31 N1 FX2_PA4
IOB1_32 N2 FX2_PA2
IOB1_33 N4
IOB1_34 P1 FX2_PA3 FATRST 17
IOB1_35 P2
IOB1_36 P3 PCIE_TDI 10
IOB1_37 P4 PCIE_TDO 10
IOB1_38 R1 FX2_PA6
IOB1_39 R2 FX2_PA5
IOB1_40 R3 FBTRST 18
IOB1_41 R4 PCIE_PRSNT2n 10
IOB1_42 T1
IOB1_43 T2
IOB1_44 T4
IOB1_45 U1
IOB1_46 U3
IOB1_47 V1
IOB1_48 V3
IOB1_49 W1
TCK W2 C_USB_MAX_TCK
TDI U2 C_USB_MAX_TDI
TDO V2 C_USB_MAX_TDO
TMS T3 C_USB_MAX_TMS

3V3 1V8 1V8 35,54 3V3 35,42,51

R474 DNI
R467 DNI
R475 DNI
R477 DNI
R434 0 EBLST_JTAG_TCK 38
R428 0 EBLST_JTAG_TDI 38
R472 0 EBLST_JTAG_TDO 38
R468 0 EBLST_JTAG_TMS 38
R473 0 FX2_PD0
R459 0 FX2_PD2
R476 0 FX2_PD3
R478 0 FX2_PD1

R452 0
38 EBLST_ENABLEN
38 EBLST_PROC_RSTn
38 EBLAST_RESERVE0
38 EBLAST_RESERVE1
35 MAXV_USB_CLK
35 MAX2toMAXV0
35 MAX2toMAXV1
35 MAX2toMAXV2
35 MAX2toMAXV3
35 MAX2toMAXV4
35 MAX2toMAXV5
35 MAX2toMAXV6
35 MAX2toMAXV7
35 MAX2toMAXV8
35 MAX2toMAXV9
35 MAX2toMAXV10
35 MAX2toMAXV11
35 MAX2toMAXV12
35 MAX2toMAXV13
FX2_RESETn
18 FBTDO

U17D EPM1270_M256FBGA
MAX II BANK4
IOB4_1 U13
IOB4_2 U14
IOB4_3 U15
IOB4_4 U16
IOB4_5 U4
IOB4_6 U5
IOB4_7 U6
IOB4_8 U7
IOB4_9 U8
IOB4_10 V14
IOB4_11 V15
IOB4_12 V16
IOB4_13 V17
IOB4_14 V18
IOB4_15 V4
IOB4_16 V5
IOB4_17 V6
IOB4_18 V7
IOB4_19 W10
IOB4_20 W11
IOB4_21 W13
IOB4_22 W14
IOB4_23 W15
IOB4_24 W16
IOB4/DEV_CLRn Y13
IOB4/DEV_OE W12
IOB4_25 W17 RJTAG_TCK
IOB4_26 W18 RJTAG_TDI
IOB4_27 W3 RJTAG_TDO
IOB4_28 W4 RJTAG_TMS
IOB4_29 W5
IOB4_30 W6
IOB4_31 W7
IOB4_32 W8
IOB4_33 W9
IOB4_34 Y1 FX2_PA7
IOB4_35 Y10 FX2_SLWRn
IOB4_36 Y11 FX2_SLRDn
IOB4_37 Y12 FATMS 17
IOB4_38 Y14 FATDI 17
IOB4_39 Y15 FATCK 17
IOB4_40 Y16 FATDO 17
IOB4_41 Y17 FBTMS 18
IOB4_42 Y18 FBTDI 18
IOB4_43 Y19 FBTCK 18
IOB4_44 Y2 FX2_PB4
IOB4_45 Y3 FX2_PB3
IOB4_46 Y4 FX2_PB2
IOB4_47 Y5 FX2_PD5
IOB4_48 Y6 FX2_PD4
IOB4_49 Y7 FX2_PD7
IOB4_50 Y8 FX2_PD6
IOB4_51 Y9 MAX_SDA

MAX_SDA

U73 SN74LVC1G17
NC 1
A 2
GND 3
Y 4 R5500 10 USB_FPGA_CLK 27
VCC 5 IO_1V8 15,20,21,22,23,25,27,~~30,40,42,74,77~~
C1563 0.1uF

PLACE NEAR CY7C68013A
3V3
C396 0.1uF C369 0.1uF C407 0.1uF C361 0.1uF C377 0.1uF C368 0.1uF C360 0.1uF C408 0.1uF

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On-Board USB Blaster II - Part 2

Logic 0 = Device JTAG Bypass
Logic 1 = Device JTAG Enable

SW3
TDA08H0SB1
A10_BYPASS
M5B_BYPASS
FMCA_BYPASS
FMCB_BYPASS
PCIE_BYPASS
MSTR0
MSTR1
MSTR2

U17B
MAX II
BANK2
EPM1270_M256FBGA

FBPRSNT_N 18
JTAG_TX
D13 GREEN_LED
R409 22.0
1V8

D14 GREEN_LED
D15 GREEN_LED
D16 GREEN_LED
SC_RX
JTAG_RX
SC_TX
R407 22.0
R406 22.0
R408 22.0

35 M5A_JTAG_TDI
35 M5A_JTAG_TDO
35 M5A_JTAG_TMS
35 M5A_JTAG_TCK
23 FTRACE_JTAG_TDO
23 FTRACE_JTAG_TDI
23 FTRACE_JTAG_TRSTn
23 FTRACE_JTAG_TCK
23 FTRACE_JTAG_TMS

MICTOR_JTAG_TRSTn 23
MICTOR_JTAG_TCK 23
MICTOR_JTAG_TMS 23
MICTOR_JTAG_TDI 23
MICTOR_JTAG_TDO 23
MICTOR_PROC_RESETn 23
M5B_JTAG_TDI 36
M5B_JTAG_TDO 36
M5B_JTAG_TMS 36
M5B_JTAG_TCK 36
FTRACE_PROC_RESETN 23
FAPRSNT_N 17

MSTR2	MSTR1	MSTR0	Mode
ON	ON	ON	BOOT
OFF	ON	ON	FMCA Master
ON	OFF	ON	FMCB Master
OFF	OFF	ON	Reserved
ON	ON	OFF	FTRACE Master
OFF	ON	OFF	GUI Test
ON	OFF	OFF	SystemMAXV Progrm Mode
OFF	OFF	OFF	ON-board UBII

U17C
MAX II
BANK3
EPM1270_M256FBGA

1V8
R424 DNI
R423 DNI
R421 DNI
R422 DNI

FTRACE_D8 23,27 Direct USB_RDn
FTRACE_D9 23,27 Direct USB_Wrn
FTRACE_D10 23,27 Direct USB_OEn
FTRACE_D11 23,27 Direct USB_RESETn
FTRACE_D12 23,27 Direct USB_EMPTY
FTRACE_D13 23,27 Direct USB_FULL
FTRACE_D14 23,27 Direct USB_SDA
FTRACE_D15 23,27 Direct USB_SCL
FTRACE_D0 23,27
FTRACE_D1 23,27
FTRACE_D2 23,27
FTRACE_D3 23,27
FTRACE_D4 23,27
FTRACE_D5 23,27
FTRACE_D6 23,27
FTRACE_D7 23,27
Direct USB D[7:0]

23,27 FTRACE_CLK
A10_JTAG_TRST 21
A10_JTAG_TDI 21
A10_JTAG_TCK 21
A10_JTAG_TMS 21
A10_JTAG_TDO 21

USB Blaster Programming Header

(uses JTAG mode only)

R458 DNI C2490 DNI
R5476 1.00k
R5477 1.00k
R5528 1.00k
R5474 1.00k
R5473 1.00k
J24
2X5_100mil
37 EBLST_PROC_RSTn
37 EBLAST_RESERVE0
EBLAST_RESERVE1 37
37 EBLST_ENABLEN
37 EBLST_JTAG_TCK
37 EBLST_JTAG_TDO
37 EBLST_JTAG_TMS
37 EBLST_JTAG_TDI
R465 0
R466 DNI

U17E
MAX II
Power
EPM1270_M256FBGA

2V5
3V3
1V8

PLACE NEAR MAX II (U25)
C382 0.1uF
C379 0.1uF
C397 0.1uF
C409 0.1uF
C378 0.1uF
C410 0.1uF
C371 0.1uF
C381 0.1uF
C370 0.1uF
C380 0.1uF

1V8 35,54
3V3 35,42,51
2V5 35,53

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PLL

69 IO_3V3

IO_3V3

C271 0.1uF C253 2.2uF

PCIE reference clock

U11 Si52112

VDD VDD2 XOUT XIN/CLKIN VSS VSS2 PLL DIFF1 DIFF1 DIFF2 DIFF2

C254 DNI C272 DNI Y2 25.00MHz

CLK_DIFF1_P 100MHz R66 0 → PCIE_REFCLK_QR0_P 8

CLK_DIFF1_N R65 0 → PCIE_REFCLK_QR0_N 8

CLK_DIFF2_P 100MHz R60 0 → PCIE_REFCLK_SYN_P 10

CLK_DIFF2_N R58 0 → PCIE_REFCLK_SYN_N 10

IO_2V5

36,68 IO_2V5

L3 742792780

C278 0.1uF C260 0.1uF C279 0.1uF C277 0.1uF C302 0.1uF

36,37,68 IO_1V8

C259 DNI C258 DNI Y6 25.00MHz

U42 Si5338A-CUSTOM

CLKIN_P CLKIN_N CLKIN I2C_LSB FDBK_P FDBK_N SCL SDA INTR CLK3B CLK3A CLK2B CLK2A CLK1B CLK1A CLK0B CLK0A RSVD_GND EPAD

VDD1 VDD2 VDDO3 VDDO2 VDDO1 VDDO0

R349 DNI R350 DNI

40,45 CLOCK_I2C_SCL

40,45 CLOCK_I2C_SDA

R149 1.00K

CLK_3An 43 CLK_3Ap 43

100MHz

25Mhz

100Mhz

CLKUSR 27

CLK_3En 43 CLK_3Ep 43

156.25MHz

CMOS

1V8_PLL C287 0.1uF C303 0.1uF L21 742792780 IO_1V8 C304 0.1uF C40 0.1uF

OSC1_CLK_SEL = HIGH selects (OSC1_CLK_SMA) SMA input

OSC1_CLK_SEL = LOW selects (OSC1_CLK_SYN) Si5356A input

IO_2V5

IO_1V8

2.5V_CLK_MUX L22 742792780

C311 0.1uF C322 0.1uF

U47 ICS83054I-5

VDD VDDQ GND CLK0 CLK1 CLK2 CLK3 OE SEL1 SEL0 Q NC1 NC2 NC3 NC4 NC5

R390 22.0 → HPS_CLK1 21

OSC2_CLK_SYN

OSC2_CLK_SMA

OSC2_HPS_CLK

J15 SMA

R370 DNI R84 DNI

C339 0.01uF

Y7 OSC_33MHZ

J16 CON2 J17 CON2

OSC2_CLK_SEL0 OSC2_CLK_SEL1

1.00K R293 1.00K R292

IO_2V5

Si5358 Programmable Oscillator Use Clock Control GUI (Defaults 156.25MHz, 156.25MHz,25MHz, 25MHz, 25MHz,100MHz, 100MHz)
I2C Address 70 HEX

I2C Address = b'1110000'

2.5V_Si516 IO_2V5

L25 BLM15AG221SN1

C463 0.1uF C439 10uF

U54 Si516_148.5M_148.35M

FS(OE) NC(SDA) NC(SCL) GND VDD CLK+ CLK- VC

36 SI516_FS

REFCLK_SDI_CP C461 0.1uF → REFCLK_SDI_P 9

REFCLK_SDI_CN C462 0.1uF → REFCLK_SDI_N 9

SI571_VCONTROL

148.5MHz

35,54 1V8

1V8 R429 10K

U51 50MHz

EN GND VCC OUT

CLKIN_50 R447 22.0 → CLK_50M_MAX 35

C373 2.2uF C372 0.1uF

IO_1V8 C41 0.1uF C305 0.1uF

IO_3V3 L28 3A, 30 Ohm FB 3.3V_VCXO C783 0.1uF C782 2.2uF

From FPGA

36 SDI_CLK148_UP

36 SDI_CLK148_DOWN

R490 180K R491 180K

R469 4.99K C419 1.0nF

C428 0.1uF

Y5 122.88 MHz

VC VDD GND OUT

41 CP1

VCXO 41

Populated with Si516.
FS Control on DIPSWITCH
FS=0: 148.35MHz
FS=1: 148.50MHz
I2C only available if Si571 is populated.

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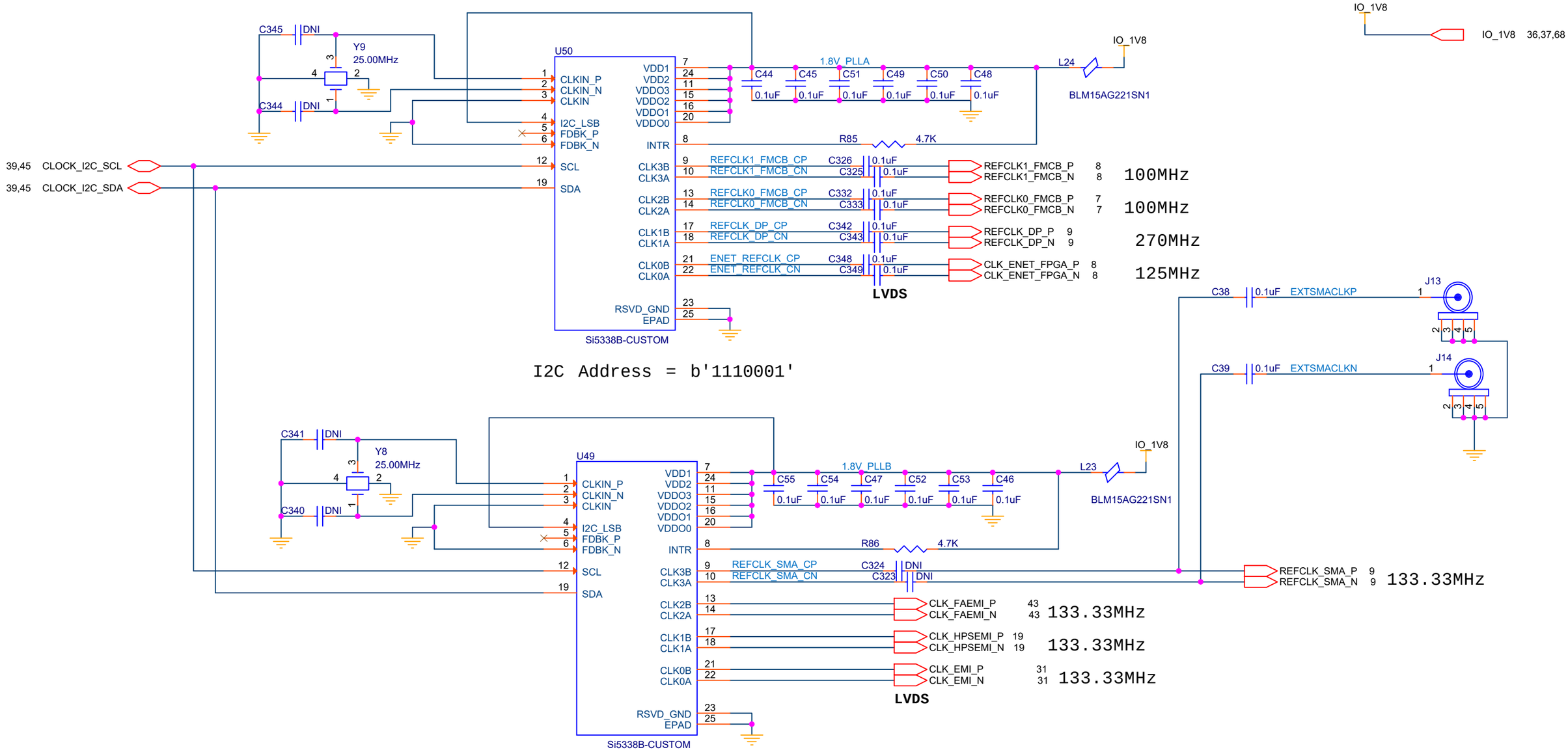
PLL (2)



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Clock Cleaner

69 IO_3V3

IO_3V3

L29 3A, 30 Ohm FB — C810 1uF, C802 0.1uF, C794 0.01uF — 3.3V_VCC1_5_6

L34 3A, 30 Ohm FB — C832 1uF, C811 0.1uF, C822 0.01uF

L30 3A, 30 Ohm FB — C821 0.01uF, C803 0.01uF

L31 3A, 30 Ohm FB

C831 0.01uF, C820 0.01uF, C793 0.01uF, C792 0.01uF, C791 0.01uF

L7 3A, 30 Ohm FB — 3.3V_VCC2

L6 3A, 30 Ohm FB — 3.3V_VCC3

L8 3A, 30 Ohm FB — 3.3V_VCC4

L33 3A, 30 Ohm FB

L32 3A, 30 Ohm FB

U26
LMK04828

10	VCC1_VCO	
17	VCC2_GC1	
21	VCC3_SYSREF	
26	VCC4_CG2	
33	VCC5_DIG	
36	VCC6_PLL1	
39	VCC7_OSCout	3.3V_VCC7
42	VCC8_OSCin	3.3V_VCC8_10
45	VCC9_CP2	3.3V_VCC9
47	VCC10_PLL2	
53	VCC11_CG3	3.3V_VCC11
64	VCC12_CG0	3.3V_VCC12
18	CS	36 SPI_CSn
37	CLKIN0p	CLK_CLN_IN_C_P
38	CLKIN0n	CLK_CLN_IN_C_N
34	CLKIN1p/FBCLKINp/FINp	LMK_CLK_IN_P
35	CLKIN1n/FBCLKINn/FINn	LMK_CLK_IN_N
43	OSCINp	OSC_IN_P
44	OSCINn	OSC_IN_N
58	CLKin_SEL0	
59	CLKin_SEL1	
31	STATUS_LD1	
48	STATUS_LD2	
5	RESET	35,36 LMK_RESET
6	SYNC	
19	SCK	36 SPI_CLK
20	SDIO	36 SPI_SDIO
11	LDObyp1	
12	LDObyp2	
65	DAP	

32	CPOUT1	
46	CPOUT2	
40	OSCOUTp	
41	OSCOUTn	
1	DCLKOUT0p	
2	DCLKOUT0n	
3	SDCLKOUT1p	
4	SDCLKOUT1n	
15	DCLKOUT2p	
16	DCLKOUT2n	
13	SDCLKOUT3p	
14	SDCLKOUT3n	
24	DCLKOUT4p	LMKR_CLK_FMC_P — R168 0 — LMK_CLK_FMC_P 43
25	DCLKOUT4n	LMKR_CLK_FMC_N — R167 0 — LMK_CLK_FMC_N 43
22	SDCLKOUT5p	LMKR_SYSREF_FMC_P — R176 0 — LMK_SYSREF_FMC_P 43
23	SDCLKOUT5n	LMKR_SYSREF_FMC_N — R175 0 — LMK_SYSREF_FMC_N 43
27	DCLKOUT6p	LMKR_CLK_FMCB_P — R174 0 — LMK_CLK_FMCB_P 43
28	DCLKOUT6n	LMKR_CLK_FMCB_N — R173 0 — LMK_CLK_FMCB_N 43
29	SDCLKOUT7p	LMKR_SYSREF_FMCB_P — R166 0 — LMK_SYSREF_FMCB_P 43
30	SDCLKOUT7n	LMKR_SYSREF_FMCB_N — R165 0 — LMK_SYSREF_FMCB_N 43
51	DCLKOUT8p	LMK_SFPCLK_C_P — C129 0.1uF
52	DCLKOUT8n	LMK_SFPCLK_C_N — C130 0.1uF — LMK_SFPCLK_P 7, LMK_SFPCLK_N 7
49	SDCLKOUT9p	
50	SDCLKOUT9n	
54	DCLKOUT10p	LMK_CLEAN_CLK_P 43
55	DCLKOUT10n	LMK_CLEAN_CLK_N 43
56	SDCLKOUT11p	LMK_SYSREF_P 43
57	SDCLKOUT11n	LMK_SYSREF_N 43
62	DCLKOUT12p	LMK_FMCCLK_C_P — C131 0.1uF
63	DCLKOUT12n	LMK_FMCCLK_C_N — C132 0.1uF — LMK_FMCCLK_P 9, LMK_FMCCLK_N 9
60	SDCLKOUT13p	
61	SDCLKOUT13n	

CP2 — C122 47pF, C121 3900pF, R198 620

C101 0.1uF, C100 0.68uF, R164 39K — CP1 39

R203 DNI, R204 DNI

J37 — LMK_CLK_P 1

J45 — LMK_SDCLK_P 1

J44 — LMK_CLK_N 1

LMK_SDCLK_N 1 — J38

R199 DNI, R191 DNI

FROM FPGA RX_CLK

43 RCLOCK_OUT_P — R183 100 — C108 0.1uF, C109 0.1uF

43 RCLOCK_OUT_N

J39 — SMA_LMK_CLK_IN — C103 0.1uF, C104 0.1uF

R721 49.9, R722 49.9

C113 0.1uF, C114 0.1uF — OSC_IN_C_P / OSC_IN_C_N — R190 100 — C115 0.1uF, C116 0.1uF

IO_3V3

L9 742792780 — 3.3V_MUX

R182 1.96K, R188 3.01K

C823 0.1uF, C824 0.1uF

J40 — LO_SMA

2.0V_VTD

C812 0.01uF, C804 0.01uF

U25

C107 0.1uF — 13 VCC, 12 VCC

C106 0.1uF — 2 D0p, 3 D0n

C112, C120 0.1uF — VCXO — 6 D1p, 7 D1n

LMK_OSC_SEL — 1 SEL0, 8 SEL1

4 VTD0, 5 VTD1

15 Q0p, 14 Q0n — MUX_OSC_IN_P / MUX_OSC_IN_N

11 Q1p, 10 Q1n

9 GND, 16 GND, 17 GND_PAD

NB6L72MNG

R189 240, R197 240

CMOS INPUT -> LVPECL OUTPUT

XJ13 — 881545-2

J33 — CON2

1.00K R11 — IO_2V5 36,68

IO_3V3

R178 10K, R177 10K

1.00K R59, R4149 1.00K

C110 10uF, C801 0.1uF

LMK_SYNC_IN — J34

D35 Green_LED — R209 820,1%

D36 Green_LED — R210 820,1%

D33 Green_LED — R207 820,1%

D34 Green_LED — R208 820,1%

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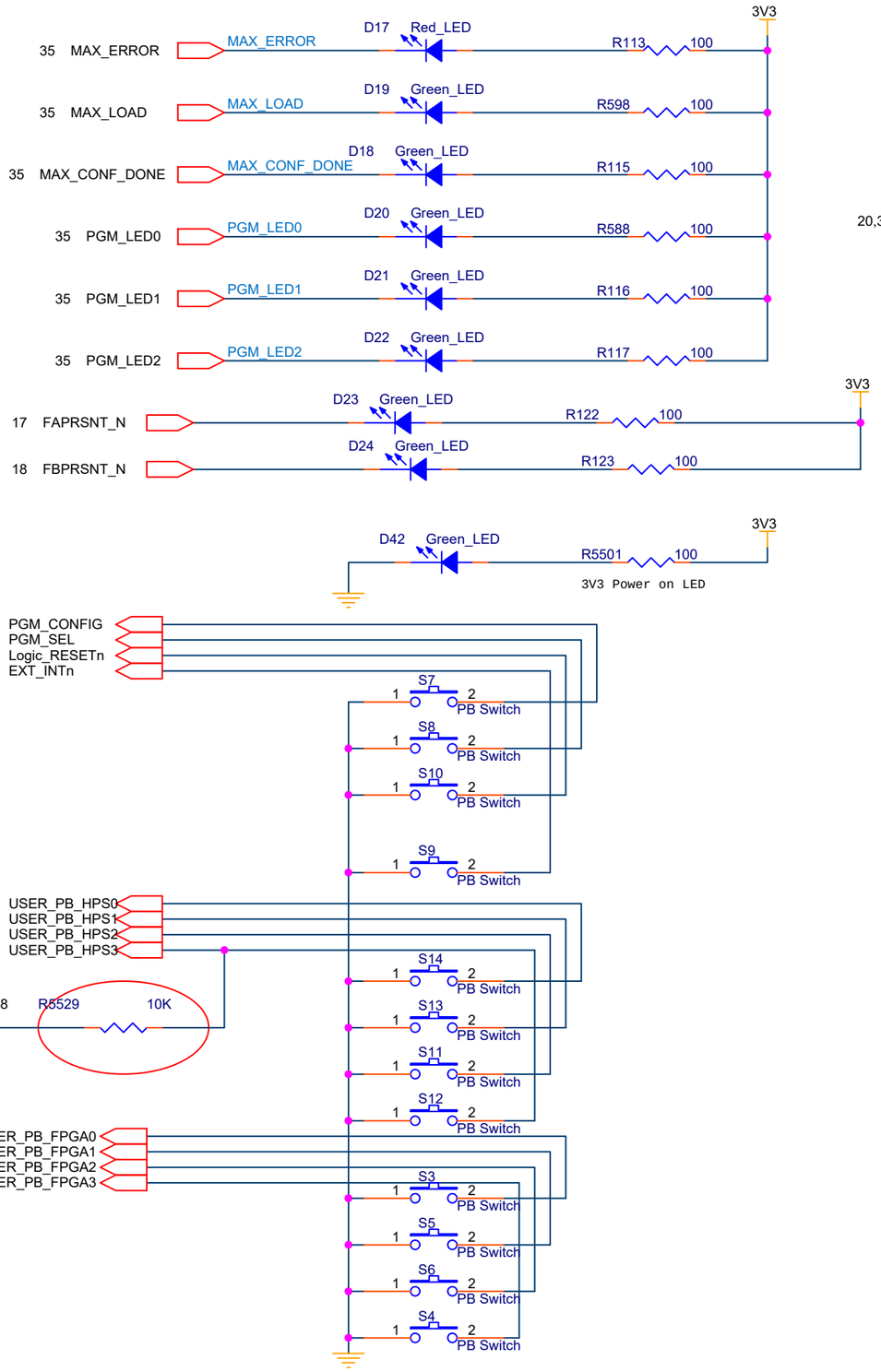
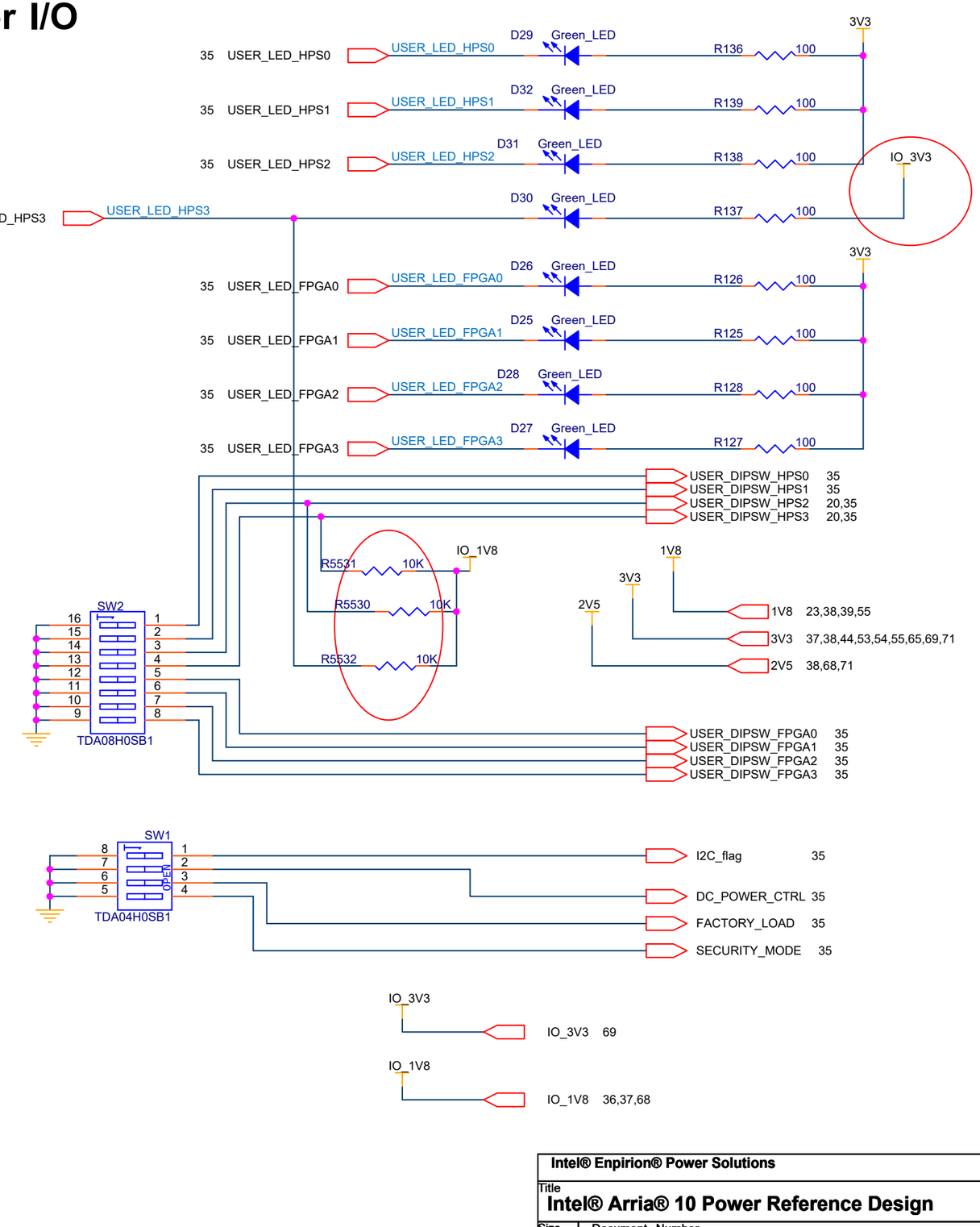
User I/O





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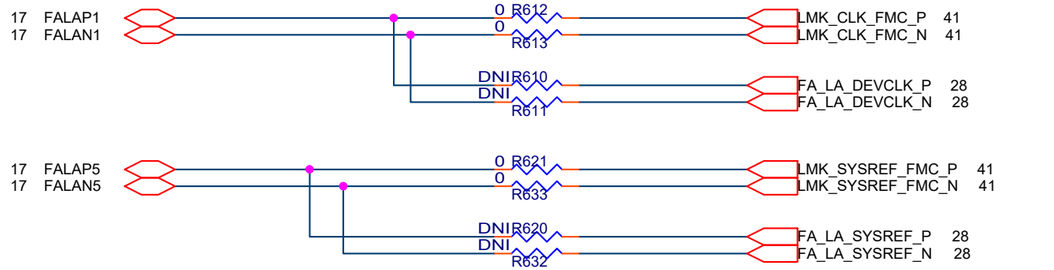
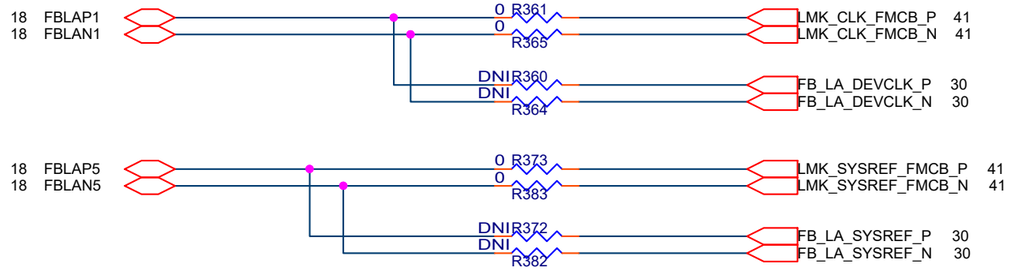
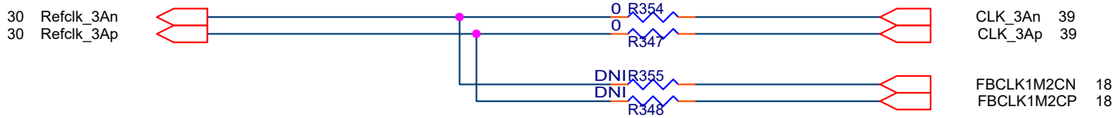
Clock Resistor Mux



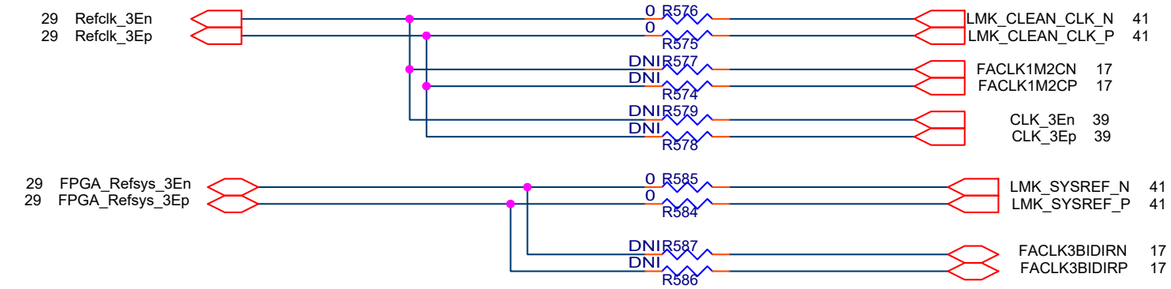
FMC A Clock MUX for TI ADC FMC card



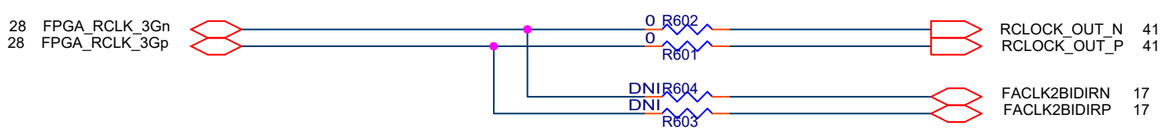
FMC B Clock MUX for TI ADC FMC card



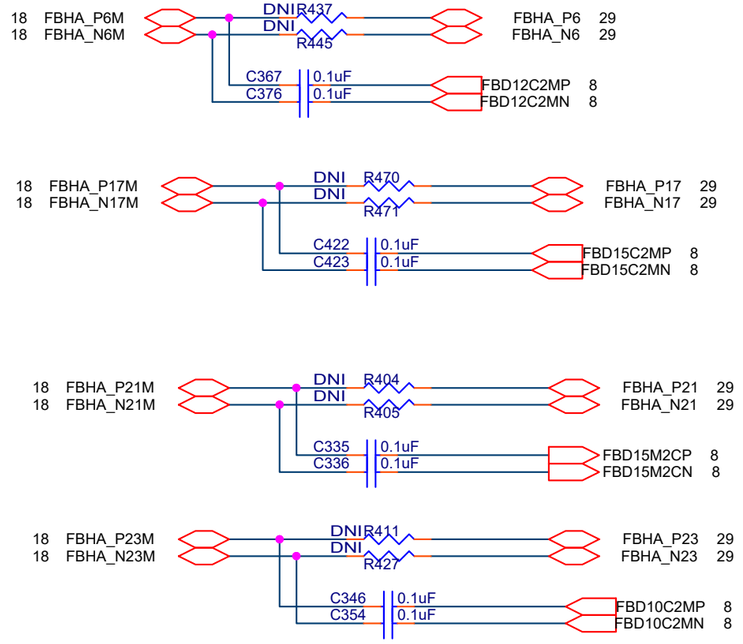
Clock MUX for 3A Bank reference clock



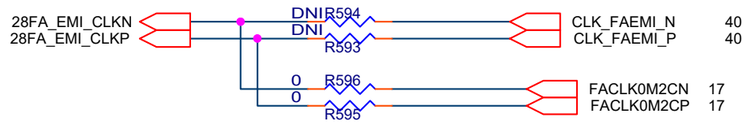
Clock MUX for 3E Bank reference clock



Clock MUX for 3G Bank reference clock



MUX for supporting Altera FMC spec



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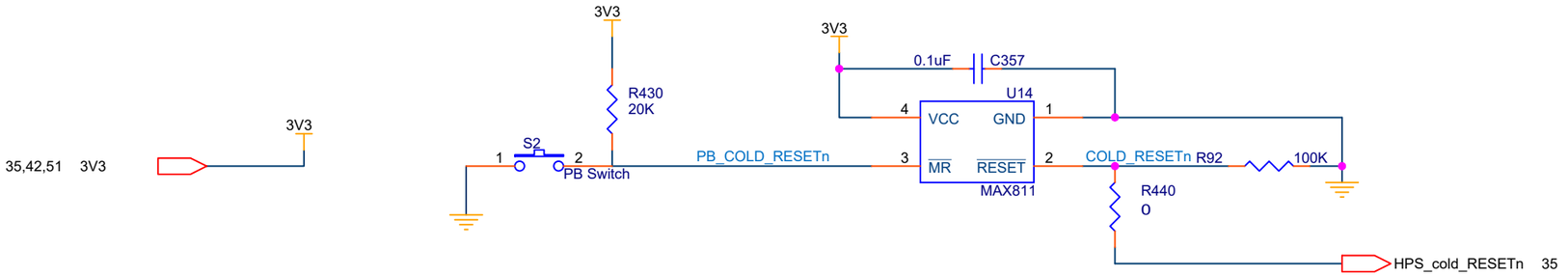
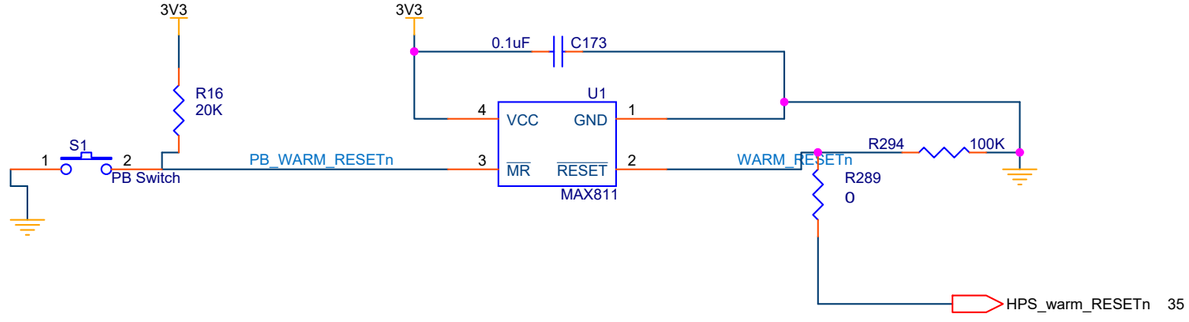
Reset Circuit

RESET CIRUIT





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I2C MUX

21 TEMPDIODE_P
21 TEMPDIODE_N
C1562 2200pf
IO_3V3
R399 200
C321 0.1uF
I2C ADDRESS:b'1001100'
U46 MAX1619
ADD1 ADD0 DXP DXN STBYn VCC NC1 NC2 NC3
OVERTn ALERTn SMBCLK SMBDATA GND1 GND2 GND3
R380 R379 4.7K 4.7K
OVERTEMPn 35
TSENSE_ALERTn 35
J28 2x5
R605 0
R614 0
PMbus connector for EM2130
PMbus_ALERTn 35,51,56,73
U48 FXMA2102UMX
A0 A1 OE VCCA GND B0 B1 VCCB
IO_5V
LT_3V3 69
IO_2V5
IO_3V3 69
IO_2V5 36,68
IO_5V 50
R376 R410 4.7K 4.7K
R387 R396 R374 R386 DNI DNI 4.7K 4.7K
R389 0
R397 0
20,35 A10_2L_SDA
20,35 A10_2L_SCL
LTSDA 71
LTSCL 71
Bus1_SDA
Bus1_SCL
R375 0
R385 0
CLOCK_I2C_SDA 39,40
CLOCK_I2C_SCL 39,40
R377 0
R402 0
EXTA_SDA 10,13,17
EXTA_SCL 10,13,17
R388 0
R398 0
EXTB_SDA 14,18
EXTB_SCL 14,18
C2350 C338 0.1uF 0.1uF
C310 C331 C330 C314 0.1uF 0.1uF 0.1uF 0.1uF
C315 C309 0.1uF 0.1uF
U43 FXMA2102UMX
PMbus_SDA_3V3 27,51,56,73
PMbus_SCL_3V3 27,51,56,73
PMBus
J35
B1 2x16 LCD BOM I2C
LCD_SCL
LCD_SDA
LCD_HEADER 0.04A
I2C ADDRESS: 0x28
R395 R394 DNI DNI
R757 R776 4.7K 4.7K
C873 0.1uF
35 A10_PMBUSDIS_N
U44 FXMA2102UMX
R401 4.7K
U45 24LC32A
A0 A1 A2 GND VCC WP SCL SDA
C320 0.1uF
I2C ADDRESS:b'1010001'
I2C ADDRESS:b'1101000'
U5 DS1339C
VCC SDA SCL GND NC1 NC2 NC3 NC4 VBACKUP SQW/INT NC5 NC6 NC7 NC8 NC9 NC10
C18 0.1uF
R29 0
R50 0
VBAT
R51 4.7K
BT1

Note to assembler: Use this resistor to attach to LCD Header (follow assembly instructions).

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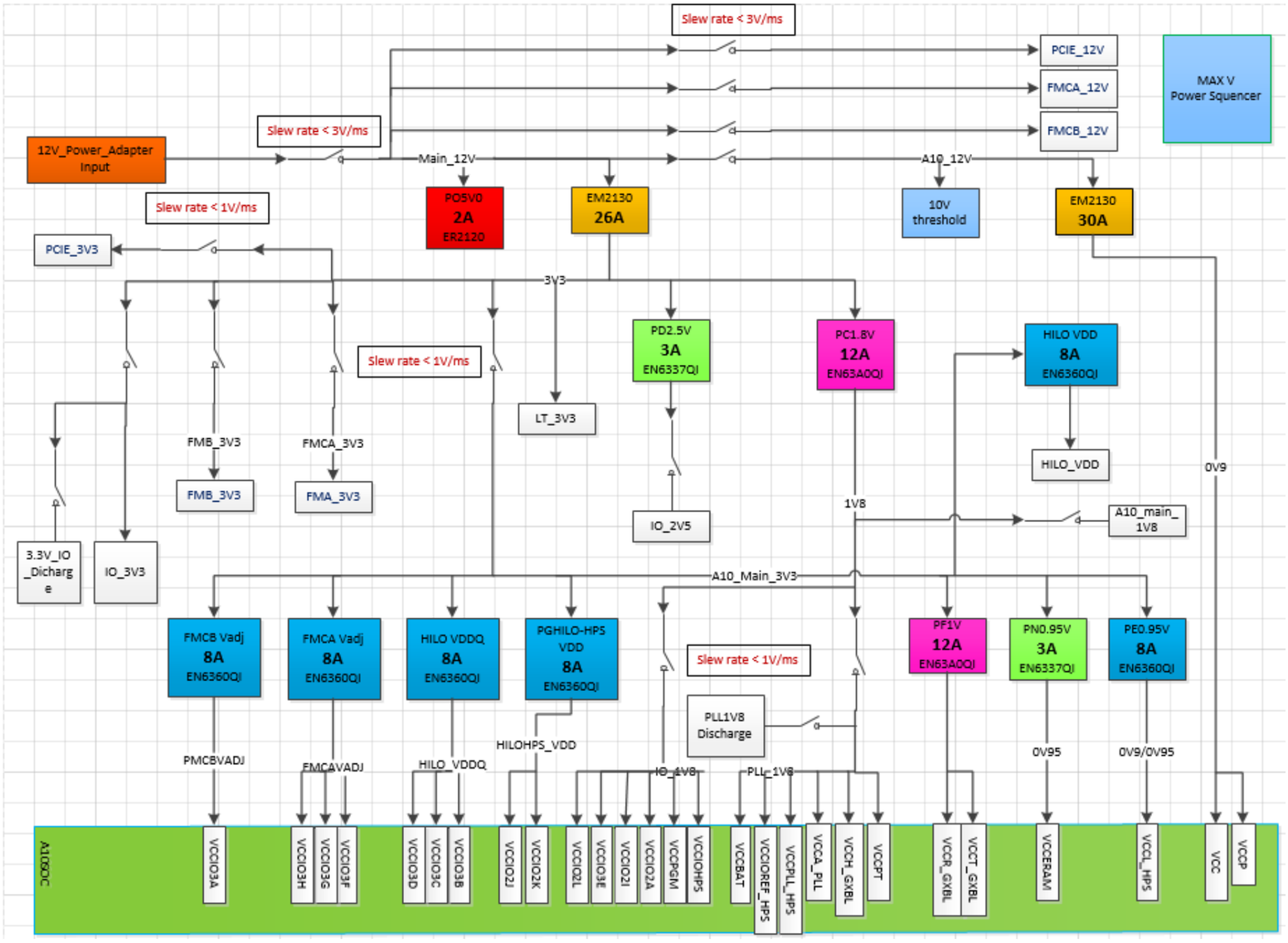
Reference Design Power Distribution Network (PDN) Diagram

(Based on Intel® Arria® 10 SoC Development Kit)



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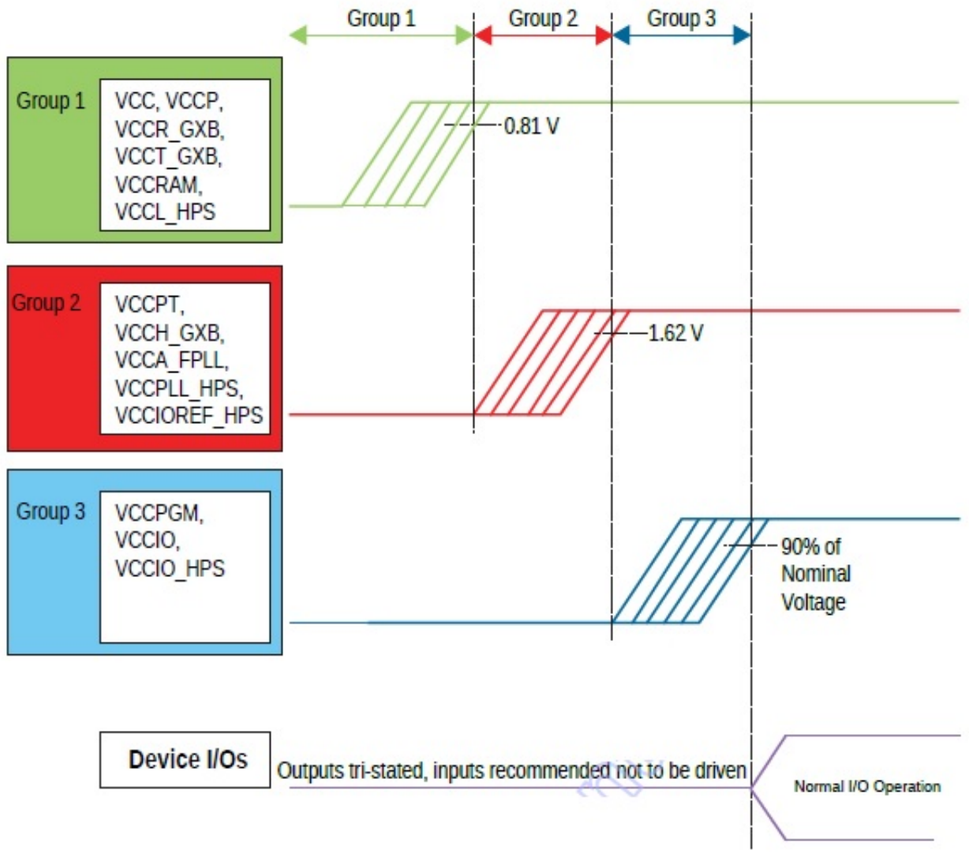
Intel® Arria® 10 SoC Power Sequence Requirements

(Based on Intel® Arria® 10 SoC Development Kit)

Figure 1: Power-Up Sequence for Arria 10 Devices



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1. If the VCC voltage level is different from VCCT_GXB, VCCR_GXB, and orVCCRAM, then ramp VCC first followed by VCCT_GXB, VCCR_GXB, and VCCRAM (In any order) within group 1
2. All Power rails must ramp completely to full rail voltage within the Tramp (0.2ms to 4ms)
3.VCCBAT (1.2-1.8V) can be powered up/down at any time and is not shown in the power sequence
4.The Power down sequence is the reverse of the power up sequence

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12V Power PMOS Switches

Input connector for 200W AC/DC adapter

J36
PD-40S
VOUT
VOUT
GND
GND
SGND
SGND
SGND
SGND
SGND
Adapter_DC_12V
R735 10
R756 10
C872 1uF
R755 49.9K
16A
Q12 Si7635DP
D41
B530C
R196 10
MAIN_GATE
SW5 SW_SLIDE_DPDT
J31
PCIe 2x4 ATX
SENSE0
SENSE1
GND
GND
GND
12V
12V
12V
12V ATX INPUT (12.5A)
R187 100K
C64 330uF 25V
C67 330uF 25V
C63 330uF 25V
C65 330uF 25V
3v/ms
R773 49.9K
R810 49.9K
R785 49.9K
Q35 DMP3098L
R786 10
C879 1uF
R774 10
Q36 DMP3098L
3v/ms
1A
FMCB_12V 18
TP114
TP113
R5354 1.00k
C899 0.1uF
R803 10K
Q42 MMBT2222A-7-F
R5353 1.00k
Q39 MMBT2222A-7-F
R775 100K
TP24
TP26
10A
MAIN_12V 27,50,51,55,68
4A
PCIE_12V 10
TP90
TP84
35 FMCB_EN
Q34 DMP3098L
R780 10
C882 1uF
R781 10
R795 49.9K
R807 49.9K
R794 49.9K
Q38 DMP3098L
R796 100K
3v/ms
R5208 49.9K
R162 49.9K
R687 49.9K
Q9 DMP3098L
R686 10
C102 1uF
R171 10
R172 100K
3v/ms
35 FMCA_EN
1A
FMCA_12V 17
TP103
TP104
R5375 1.00k
C898 0.1uF
R808 10K
Q41 MMBT2222A-7-F
R5374 1.00k
Q37 MMBT2222A-7-F
R5214 1.00k
C777 0.1uF
R685 10K
Q30 MMBT2222A-7-F
R5213 1.00k
Q31 MMBT2222A-7-F
35 PCIE_EN

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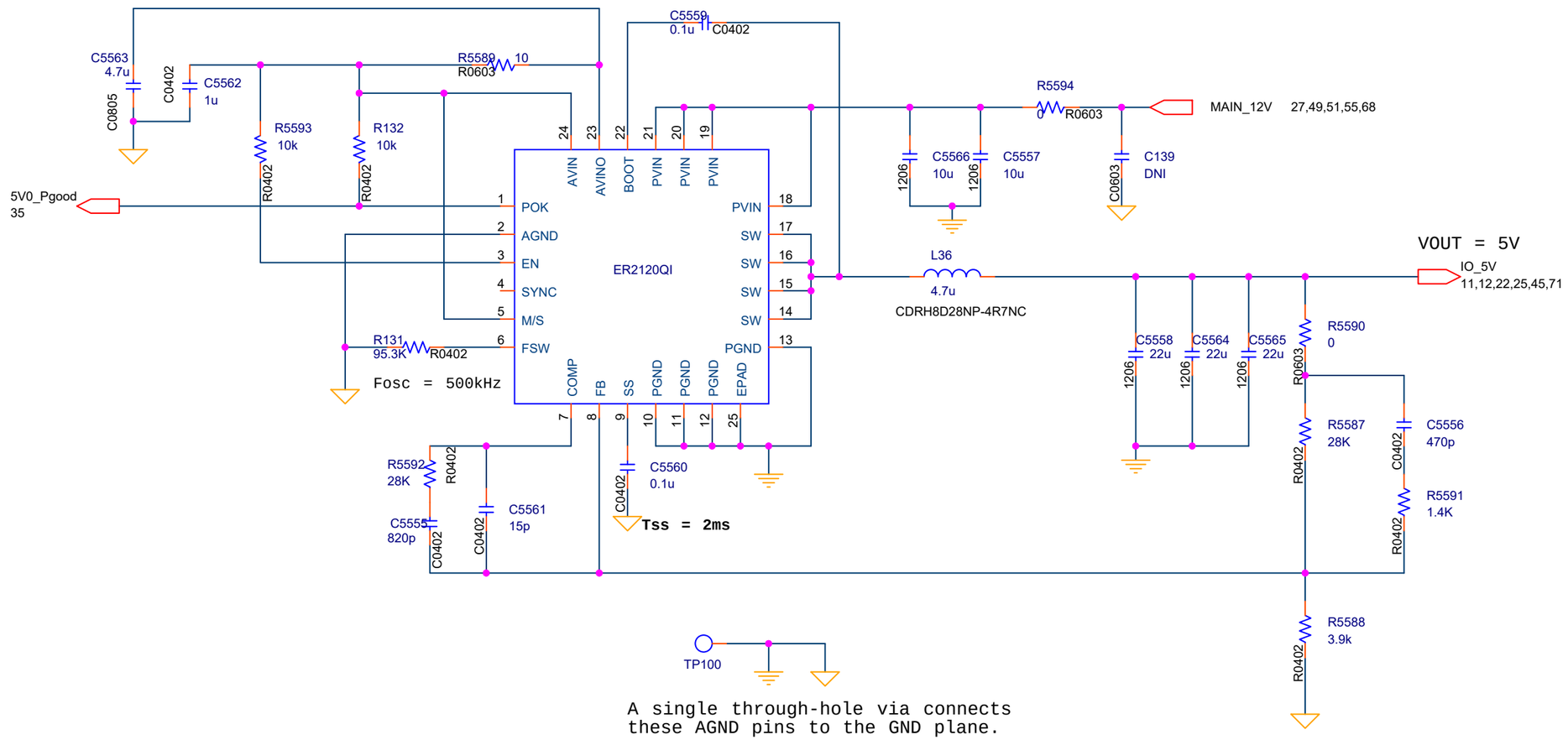
12V to 5V Converter



A single through-hole via connects
these AGND pins to the GND plane.

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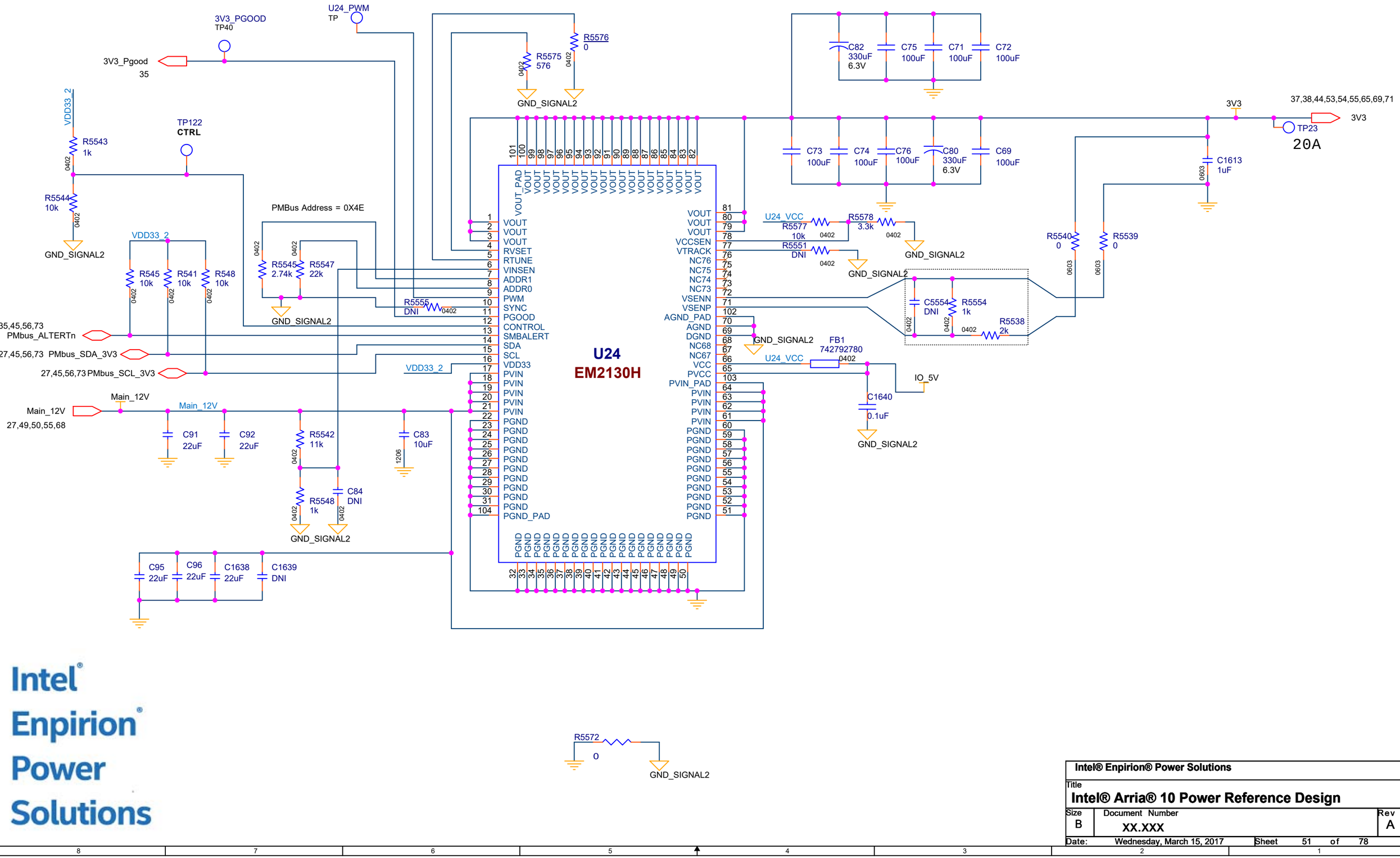
12V to 3V3 Converter



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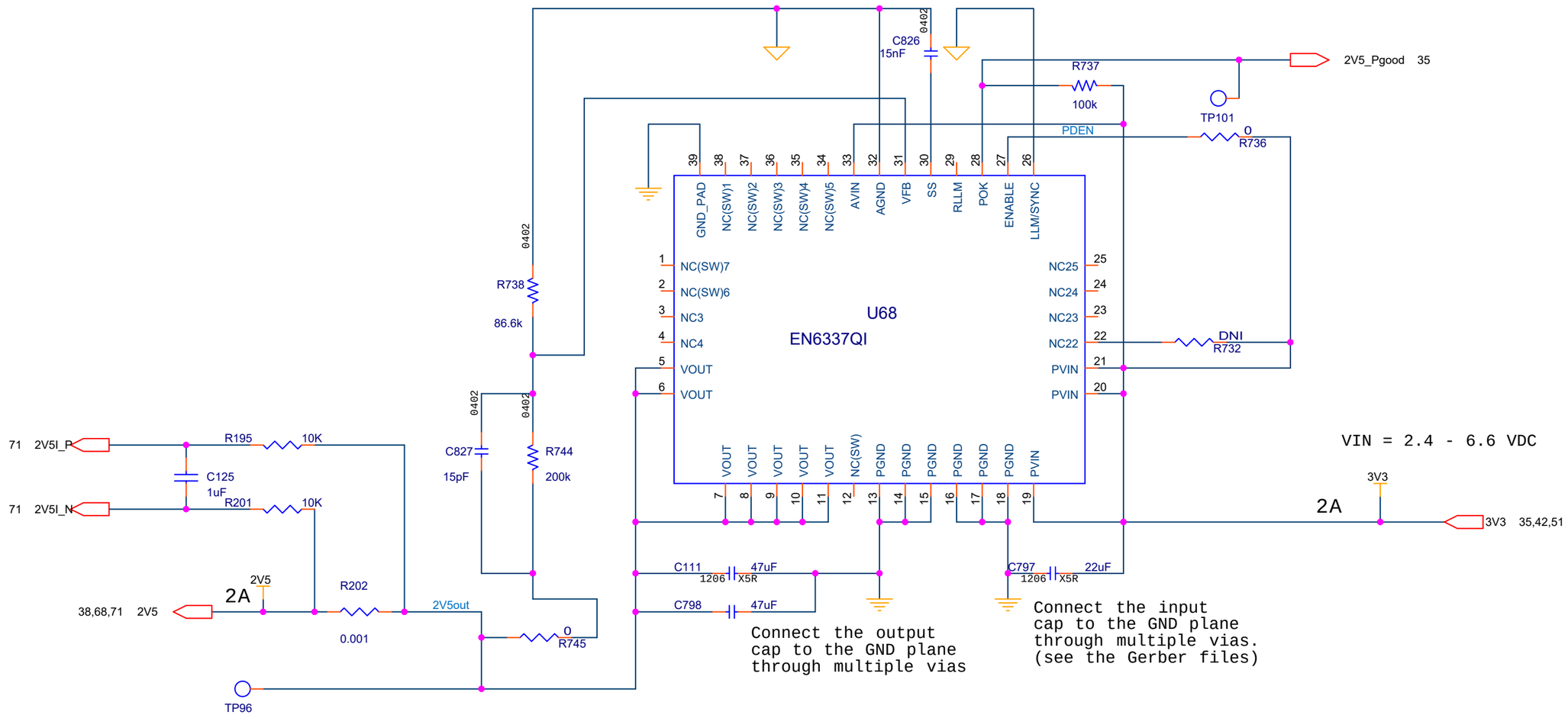
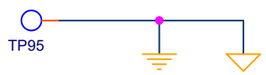
3V3 to 2V5 Converter





A single through-hole test point connects the AGND pin to the GND plane.

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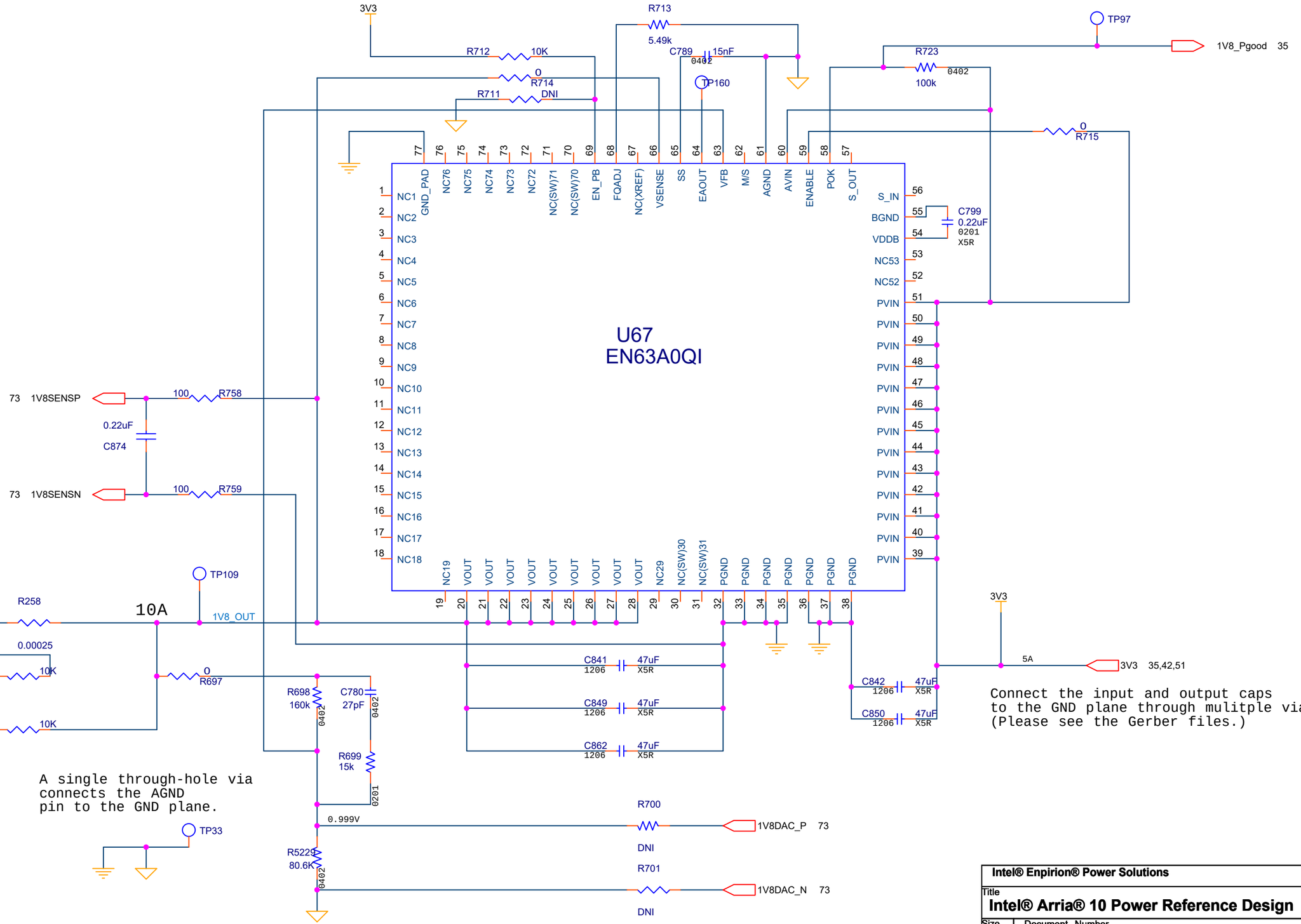
3.3V to 1.8V Converter



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Intel® Arria® 10 12V,3V3 and 1V8 PMOS Switches

27,49,50,51,68 9A
49 MAIN_12V
MAIN_12V
Q10
Si7635DP
3
2
1
5
6
7
8
4
R681
49.9K
C774
1uF
R682
10
A10_12V
3.5A
A10_12V 56,73
TP87
TP89
R53
25.5K
R680
100K
C
B
Q29
MMBT2222A-7-F
E
R694
35 A10_EN
10K
C779
0.1uF
R693
10K
J58
1
2
CON2
TP88
J58 need be shorted if MAXV is not programmed
R54
49.9
R5491
1.00k
3V3
R55
10K
R52
10K
U39
INA+
INB-
GND
OUTA
OUTB
VDD
TPS3700
C20
0.1uF
10V_Fail_n 35
10V_good 35
TP45
TP44
Typical 12V good threshold voltage is 10.62V.
Typcial 12V bad threshold voltage is 10.11V
35,42,51 3V3
3V3
Q27
8
7
6
5
3
2
1
4
SiRA00DP
10A
A10_main_3V3 58,59,60,62,63,64,66,67
TP68
TP69
MAIN_12V
R608
100K
R597
1.00k
C599
0.01uF
C
B
Q28
MMBT2222A-7-F
E
Q44
8
7
6
5
3
2
1
4
SiRA00DP
1V8
35,54 1V8
MAIN_12V
R277
100K
R273
100K
R278
1.00k
C894
0.01uF
R607
10K
C
B
Q40
MMBT2222A-7-F
E
C
B
Q46
MMBT2222A-7-F
E
C1560
100uF
6.3V
C1561
100uF
6.3V
10A
A10_main_1V8 68
TP42
TP37

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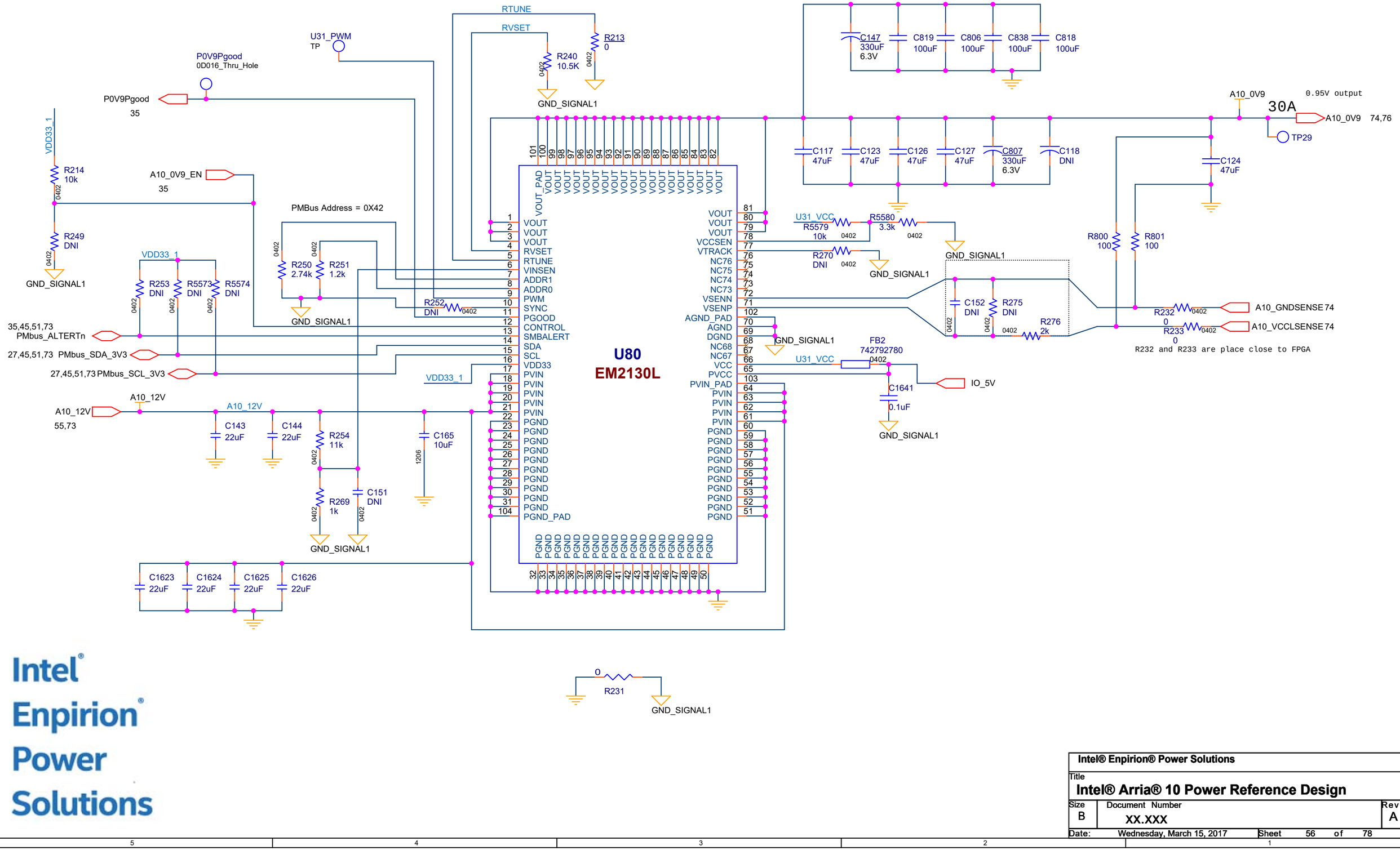
12V to 0V9 Converter



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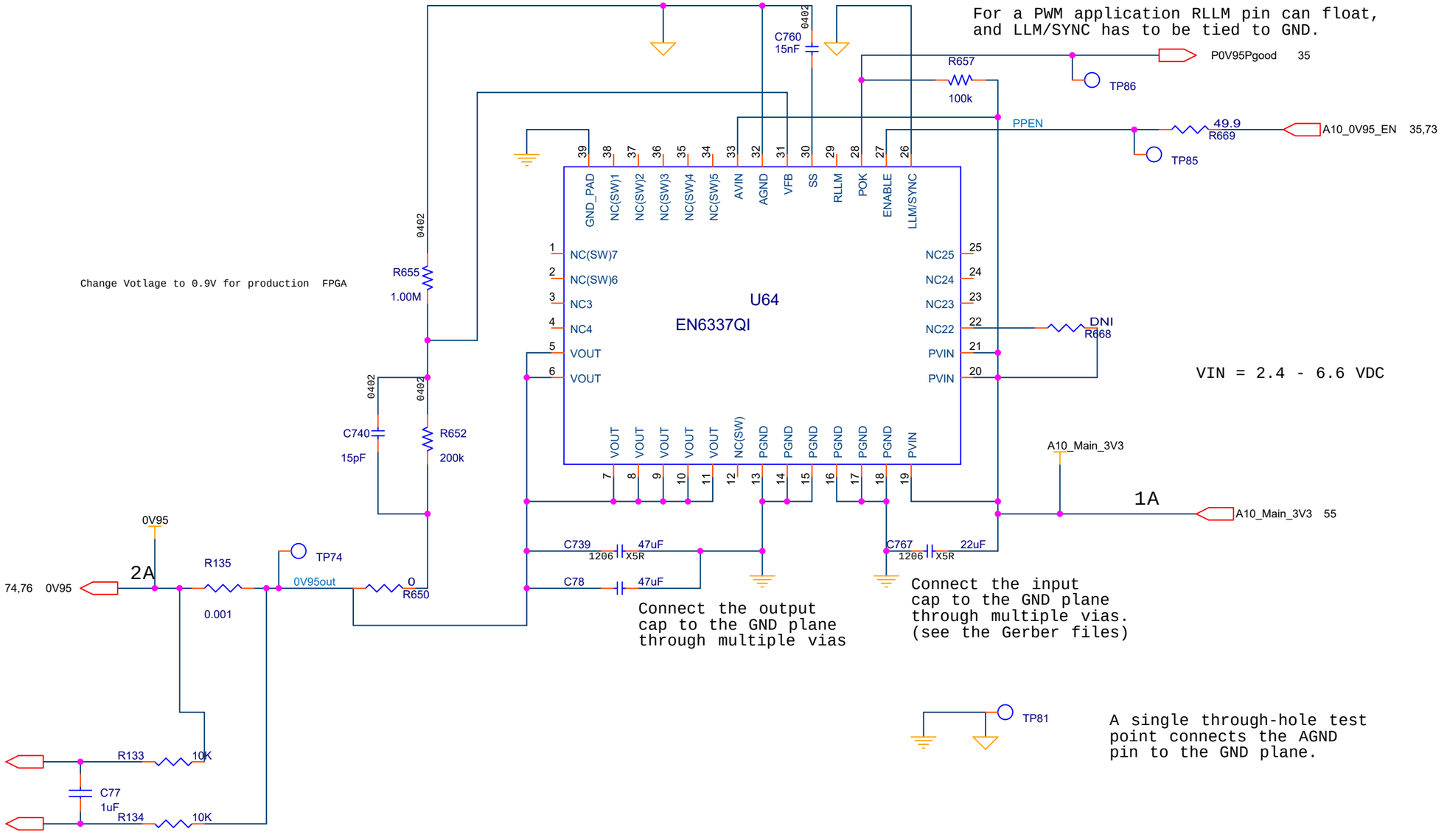
3.3V to 0.9V Converter



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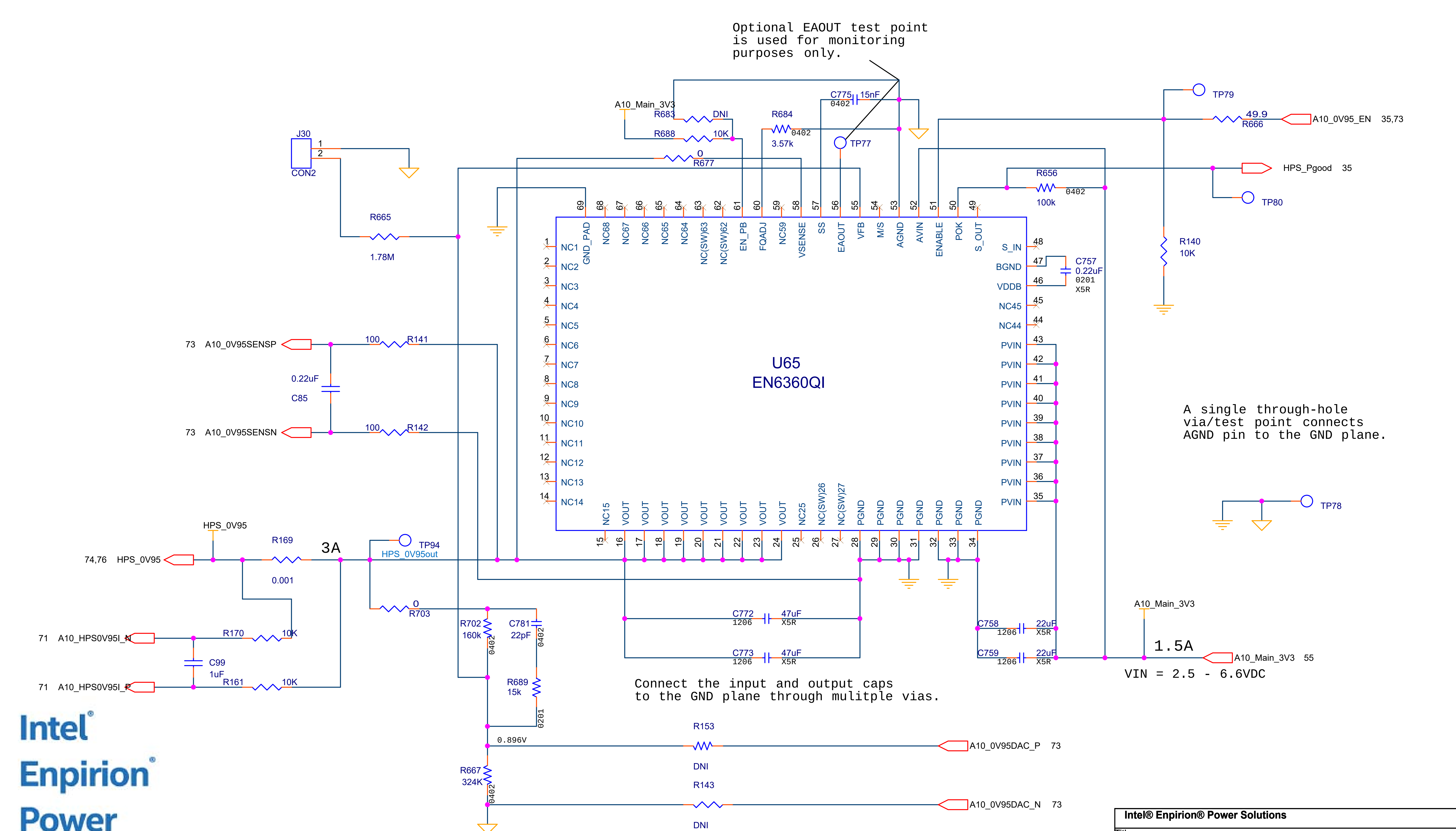
3.3V to 0.9V Converter (HPS Core)



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3.3V to 1.0V Converter

A single through-hole via connects the AGND pin to the GND plane.

U56
EN63A0QI

Feedback network configured for 3.3Vin /1.0Vout

Update the value to 226K from 240K for 1.03V output

+-15% range

Connect the input and output caps to the GND plane through mulitple vias. (Please see the Gerber files.)

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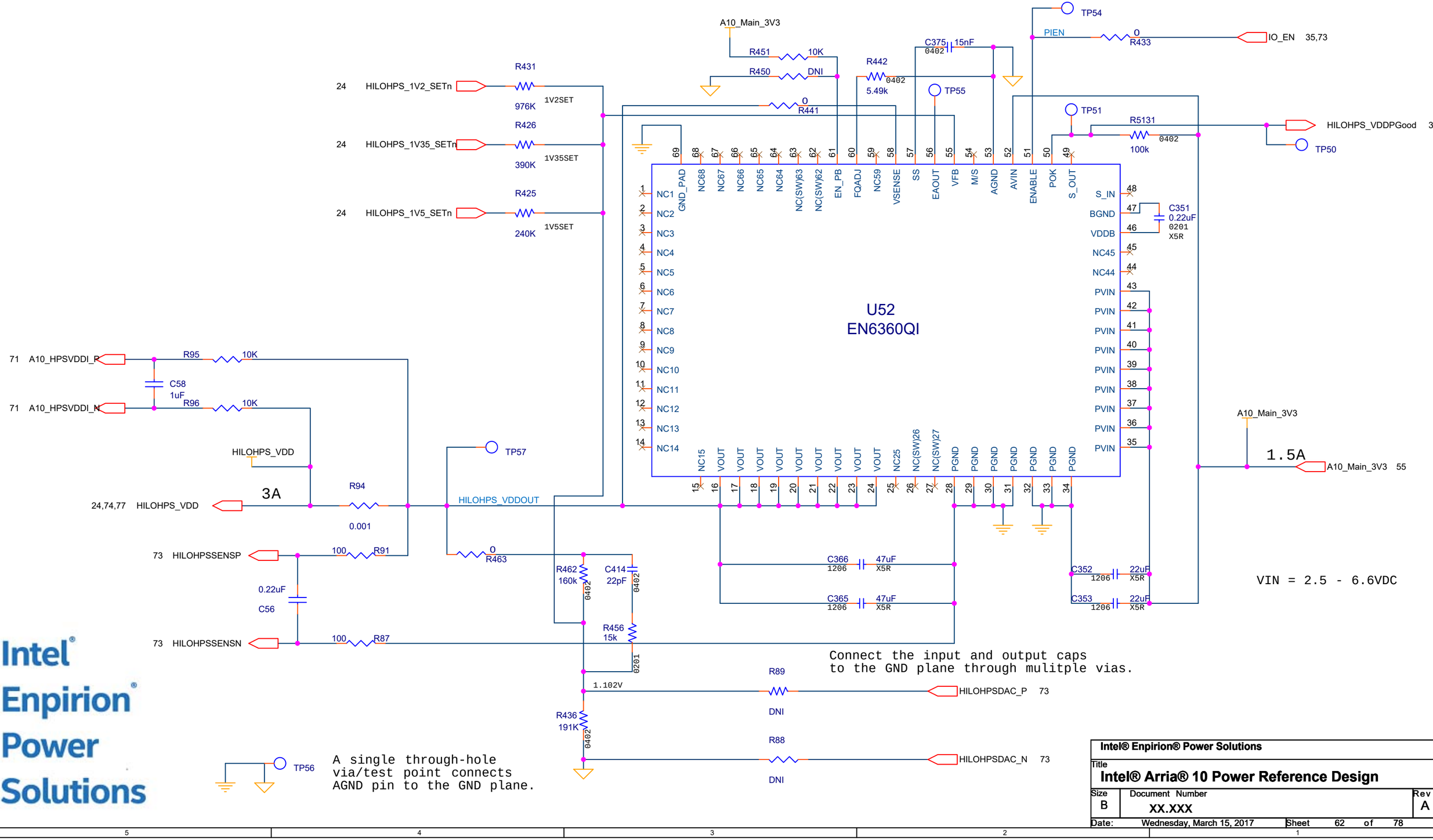
3.3V to HPS HILO VDD Converter



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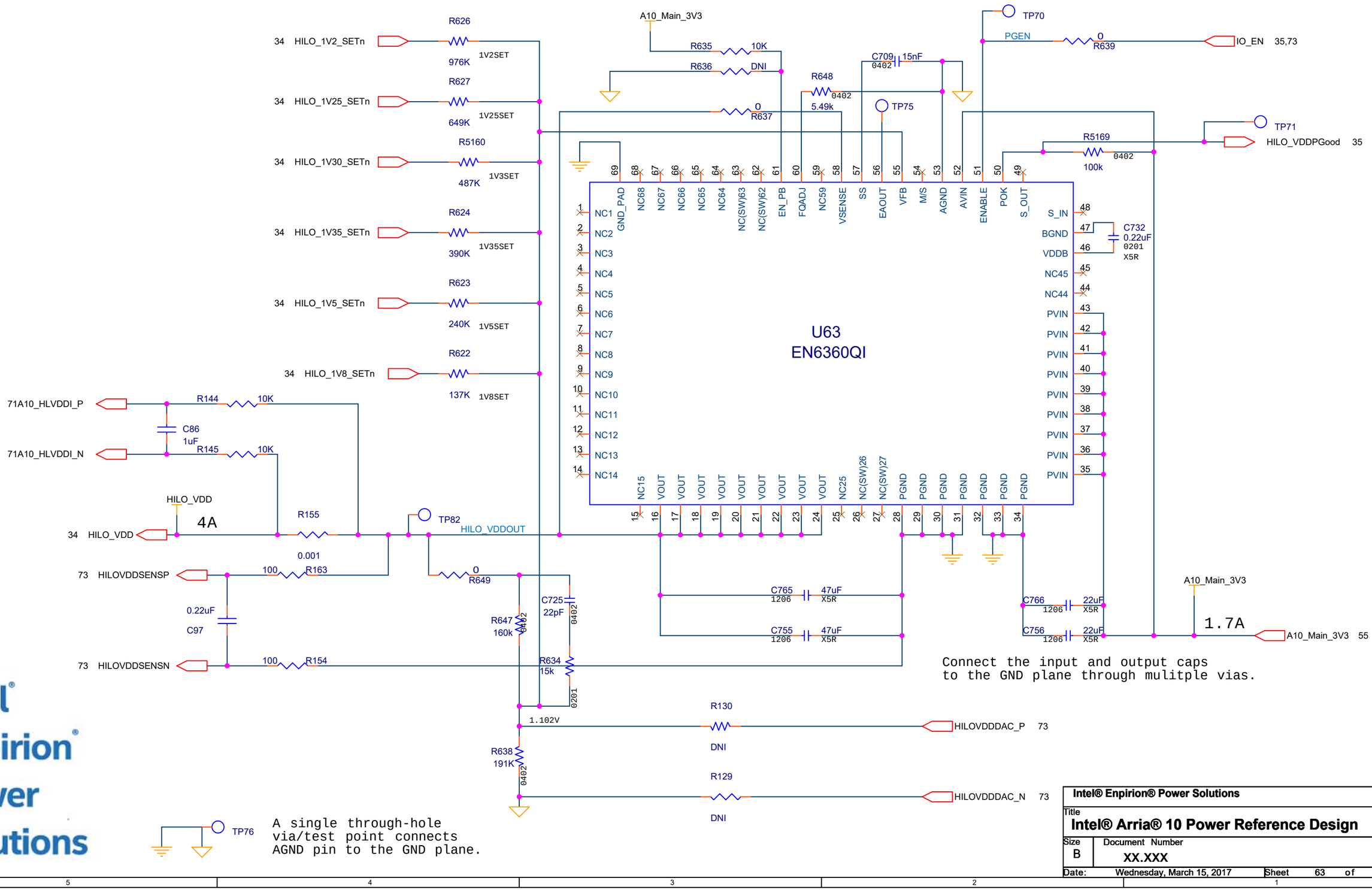
3.3V to HILO VDD Converter



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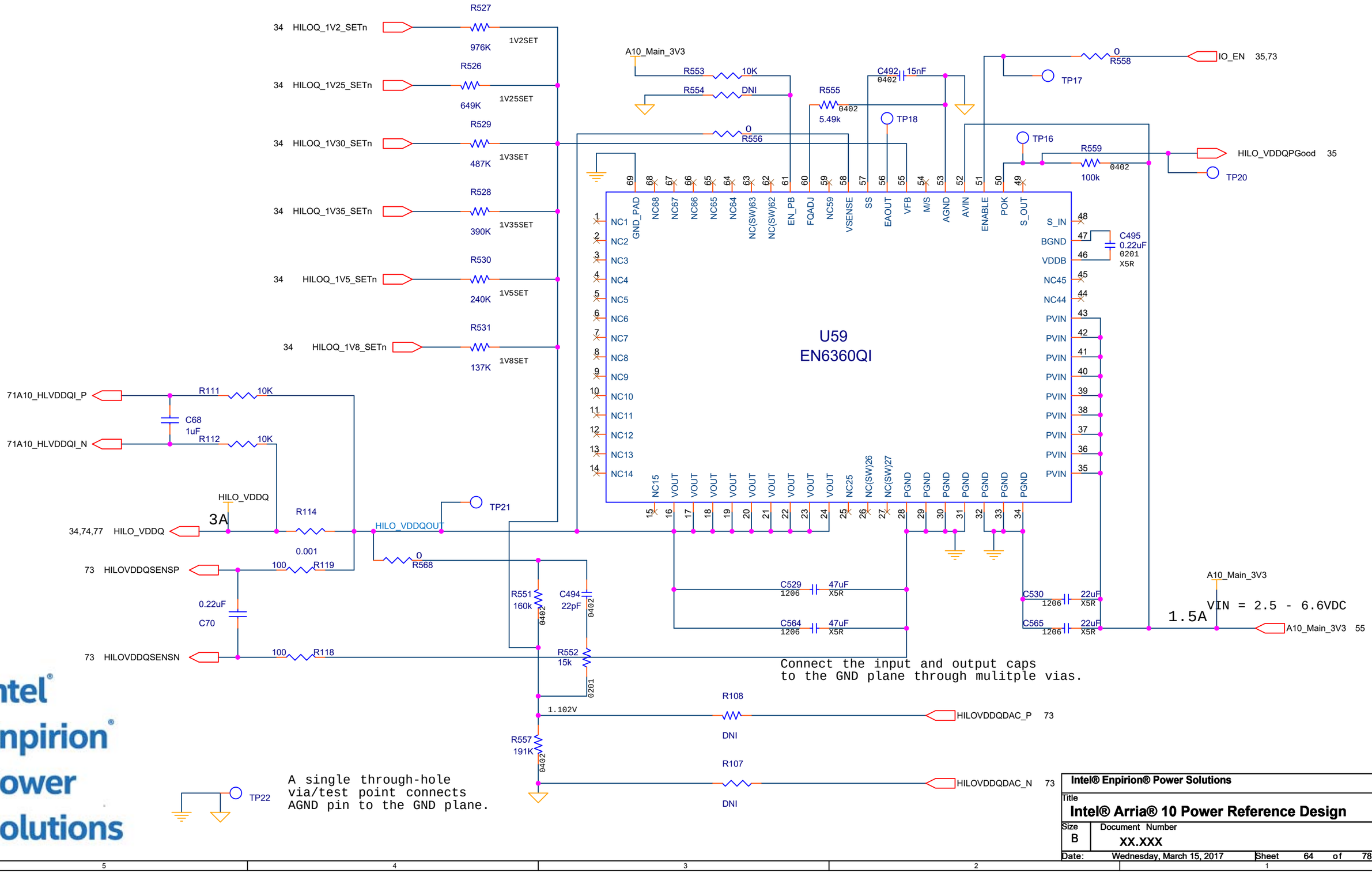
3.3V to HILO VDDQ Converter



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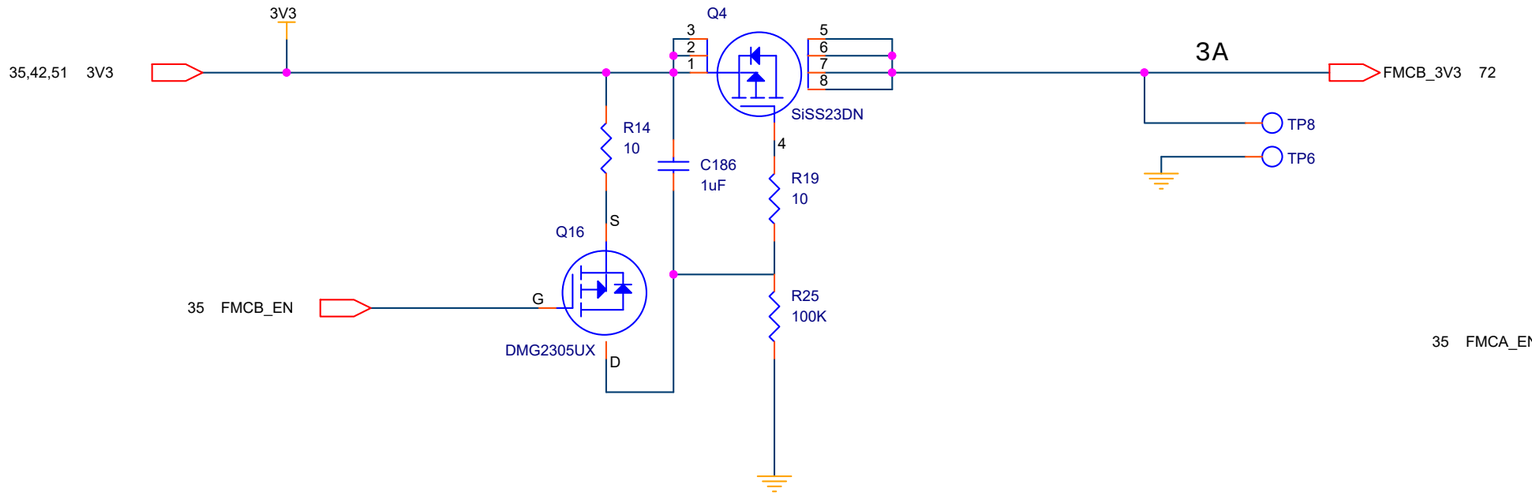
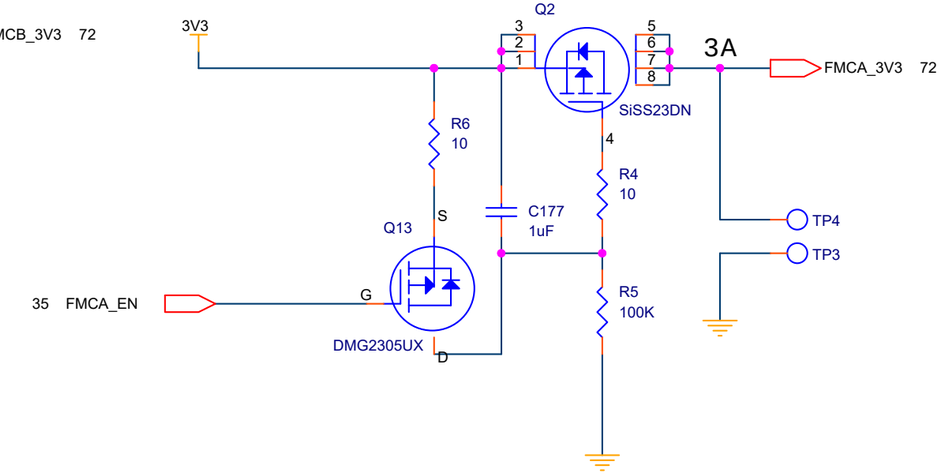
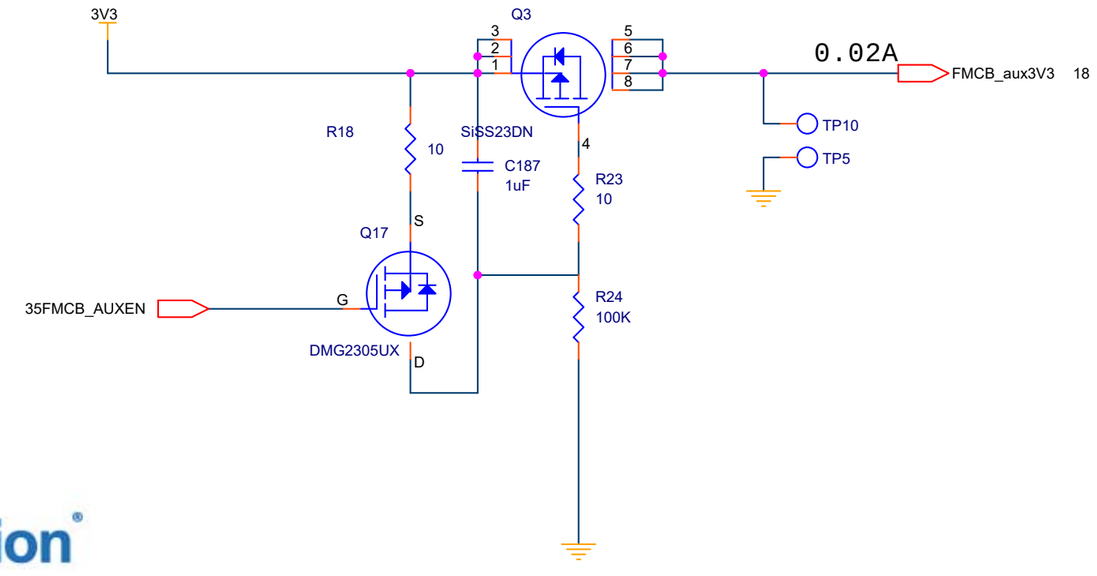
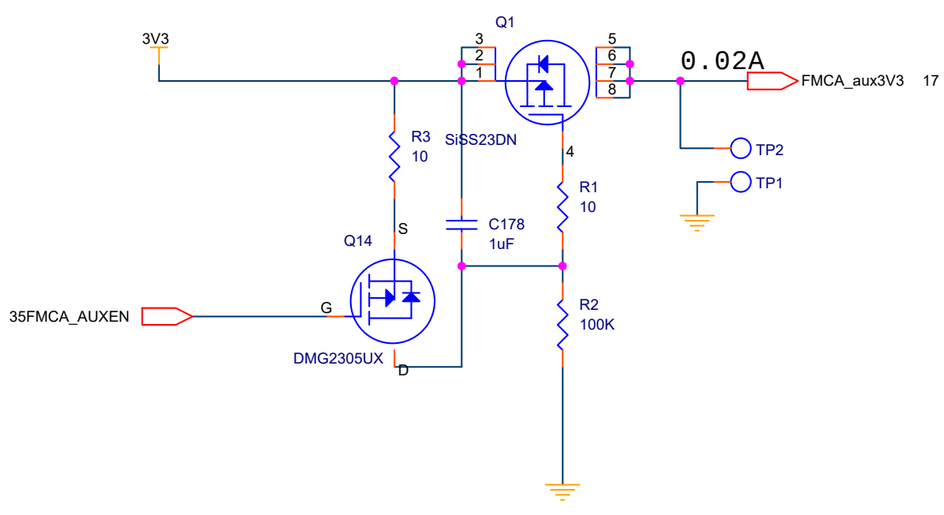
FMC 3.3V PMOS Switches









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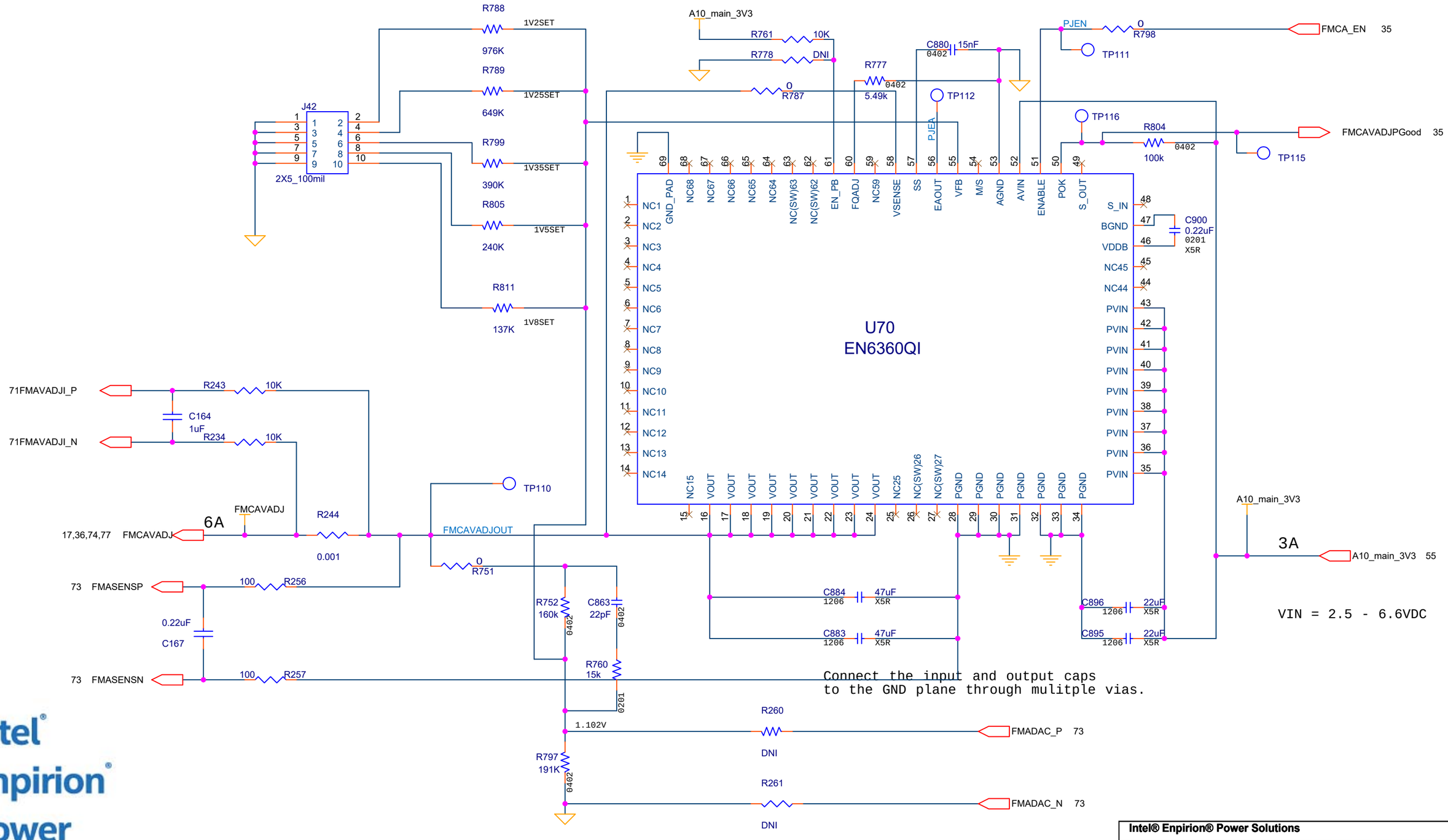
3.3V to FMC A VADJ Converter



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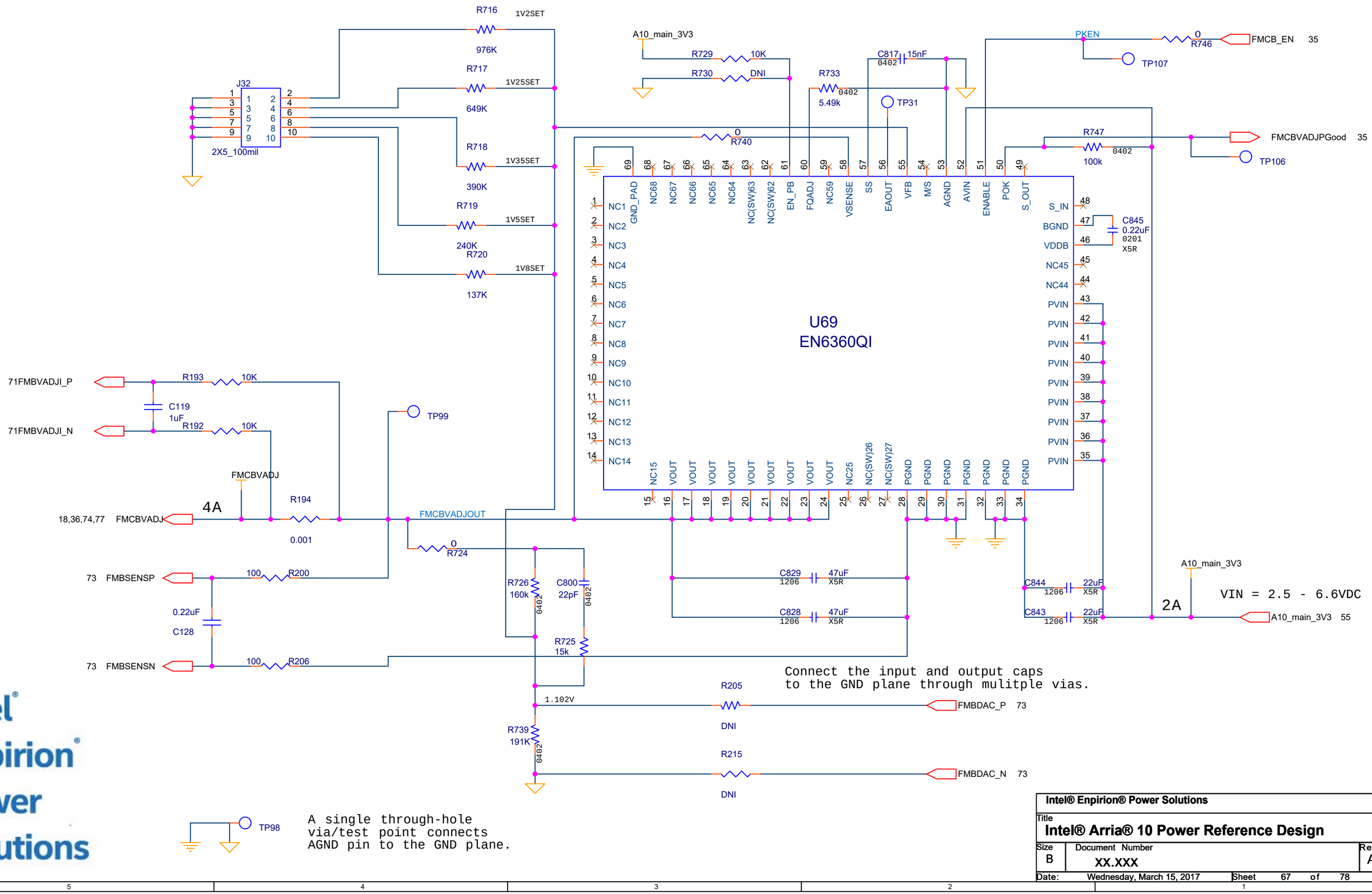
3.3V to FMC B VADJ Converter



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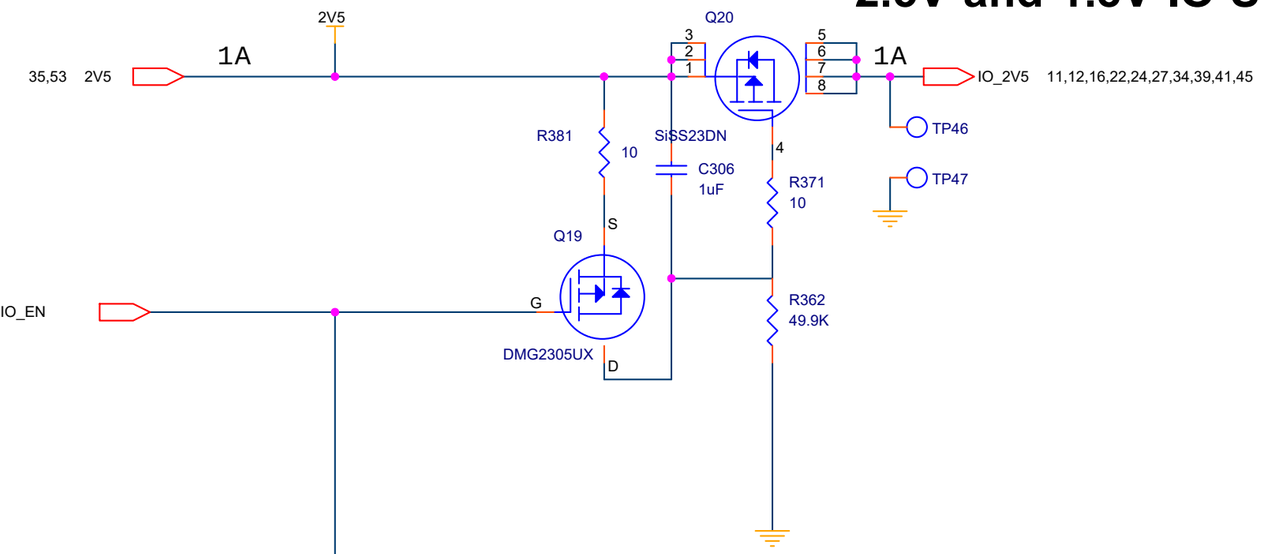
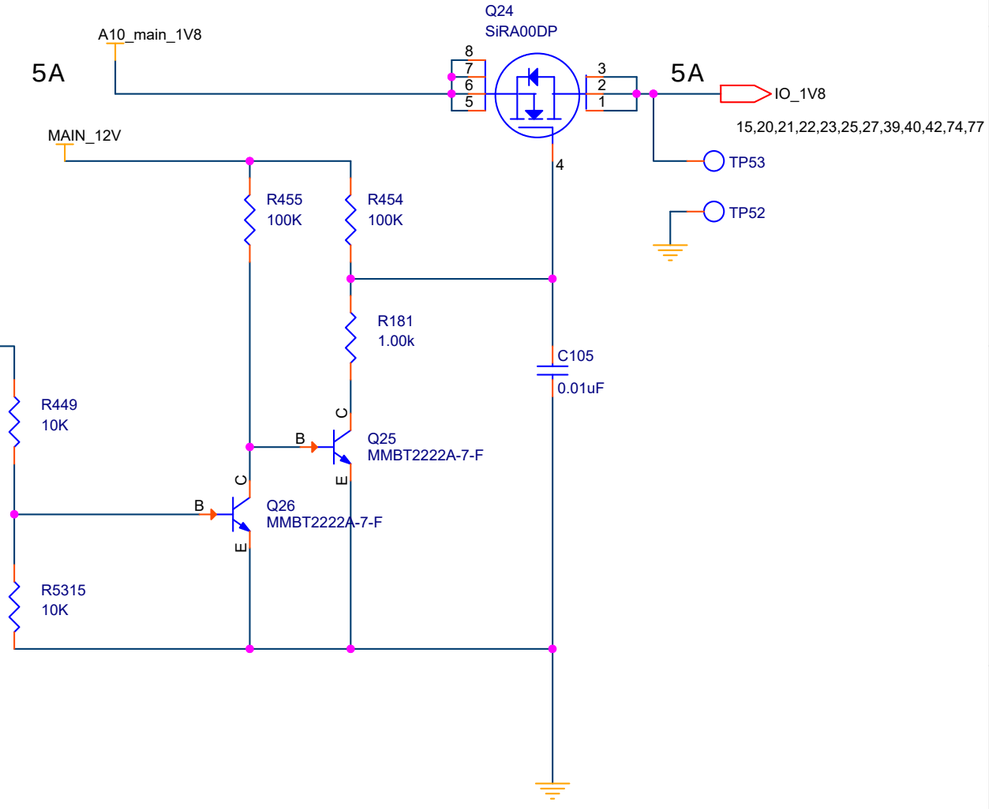
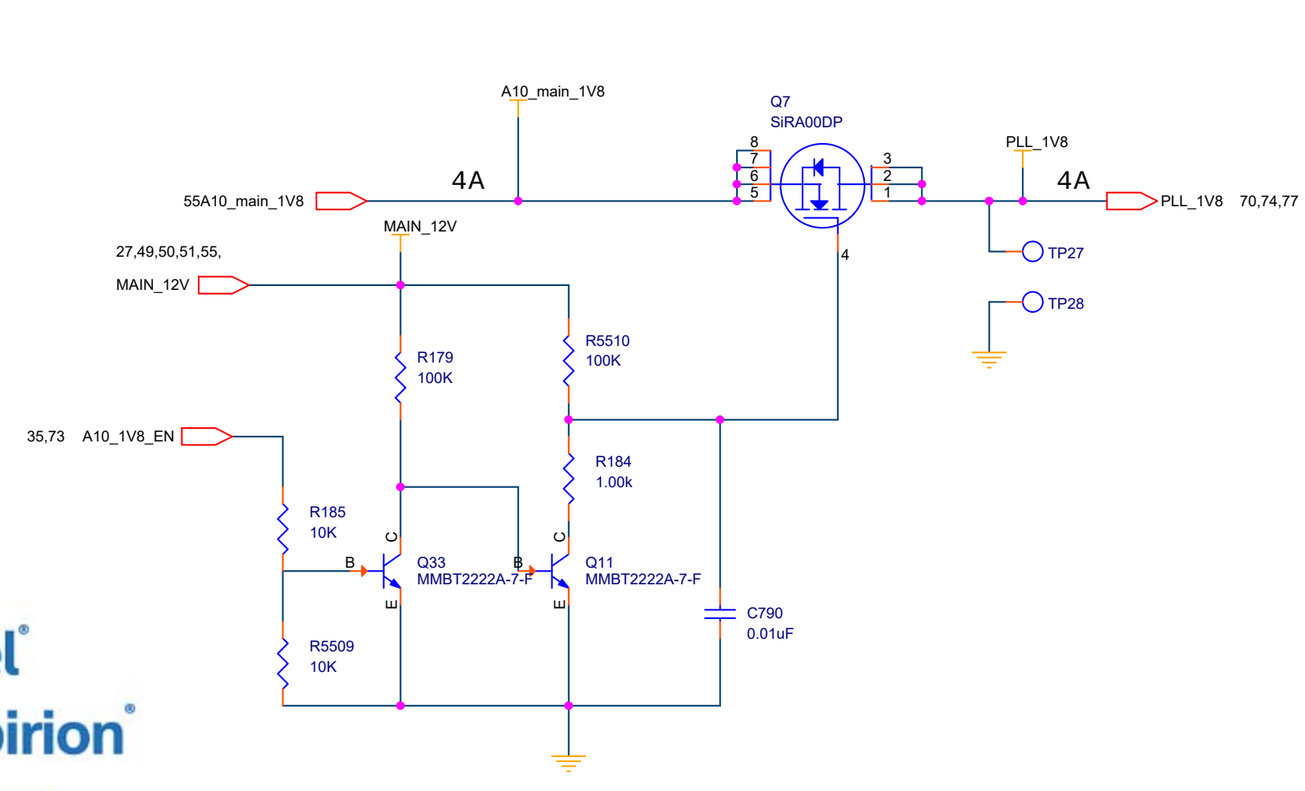
2.5V and 1.8V IO Switches







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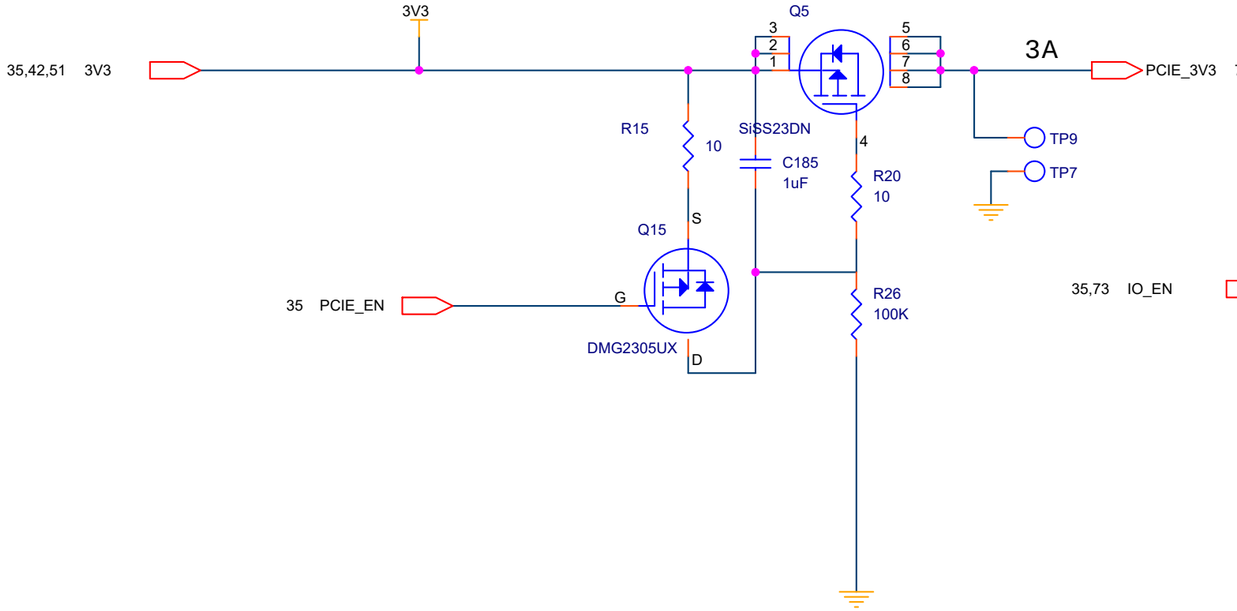
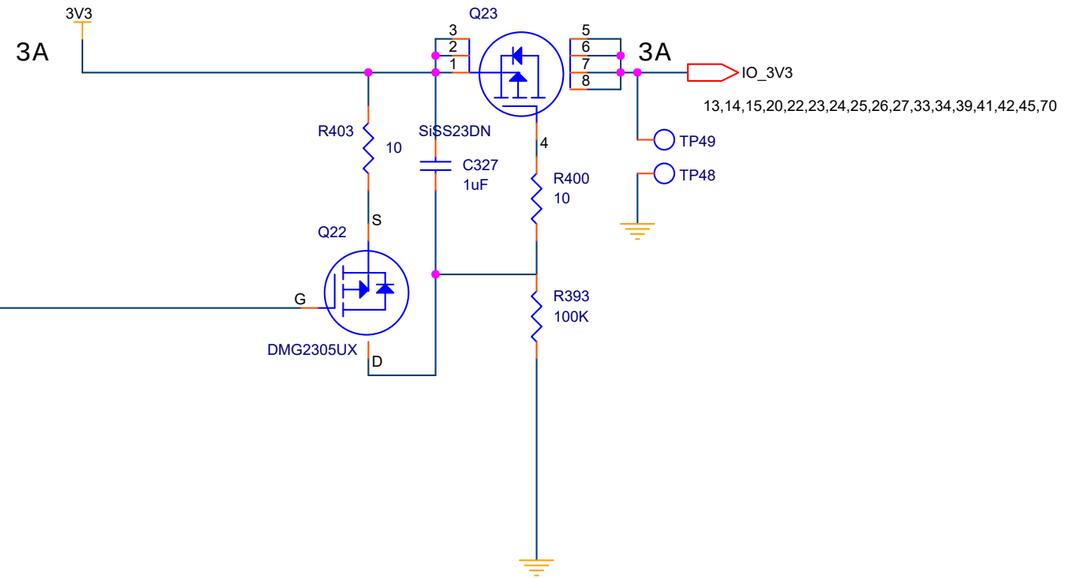
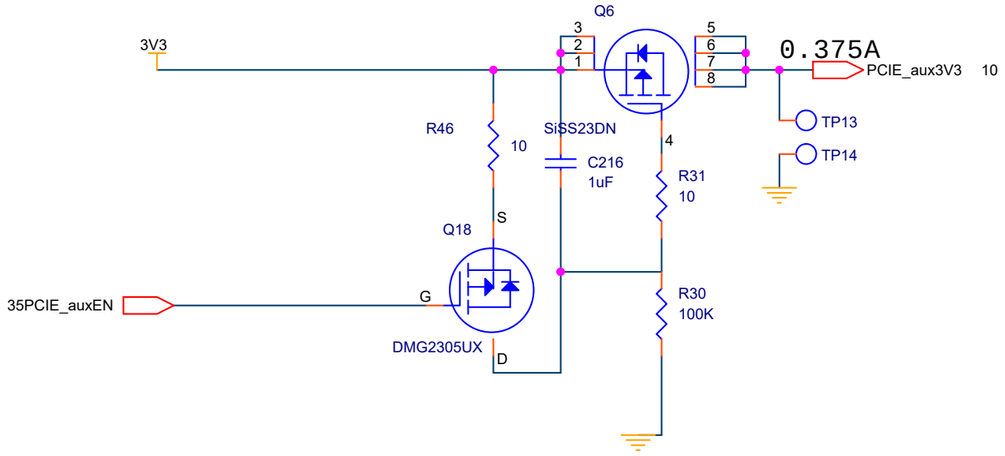
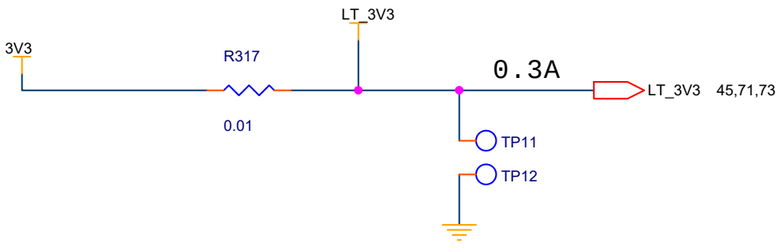
3.3V IO Switches









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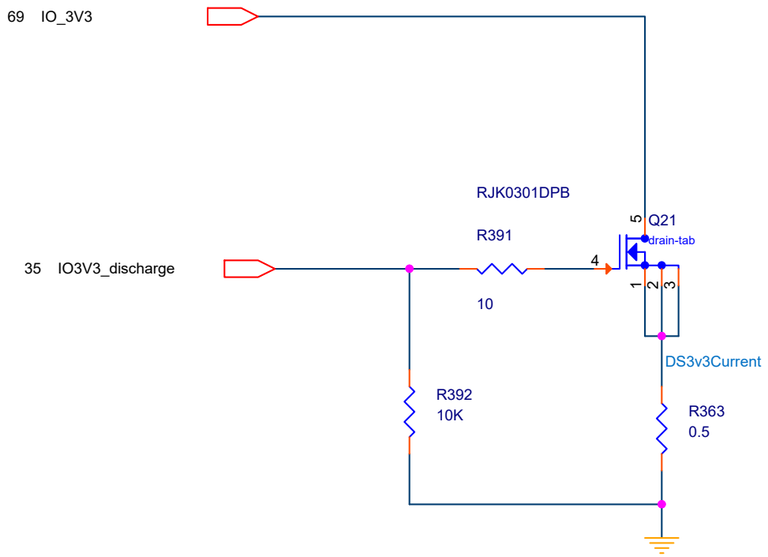
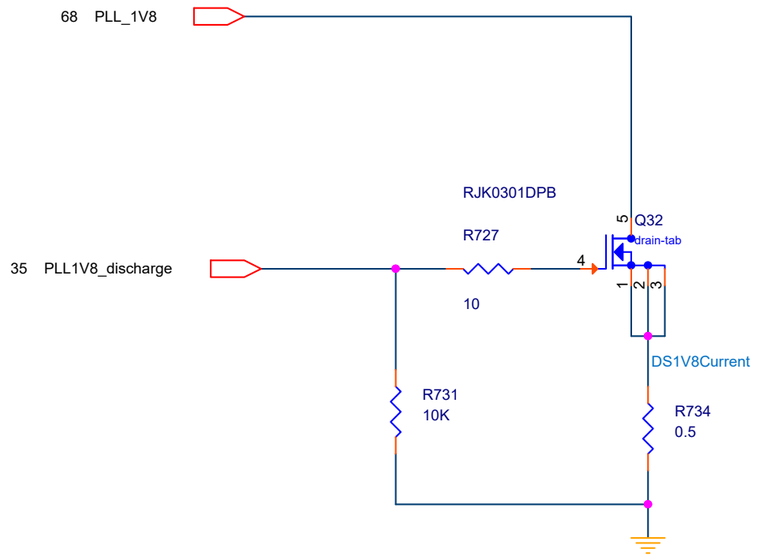
3.3V and 1.8V Discharge Load





50us Discharge time

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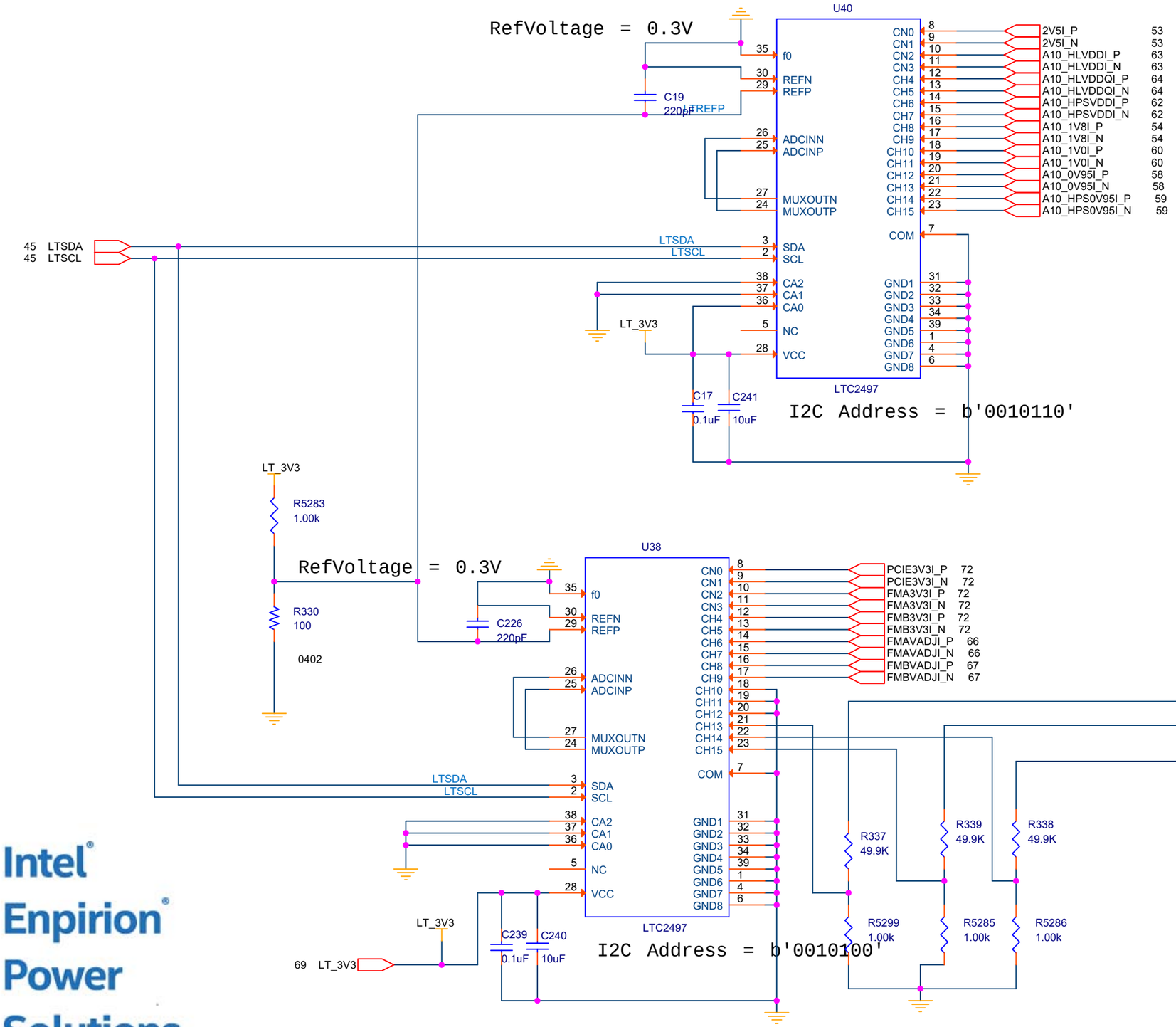
I2C Current ADC (A)



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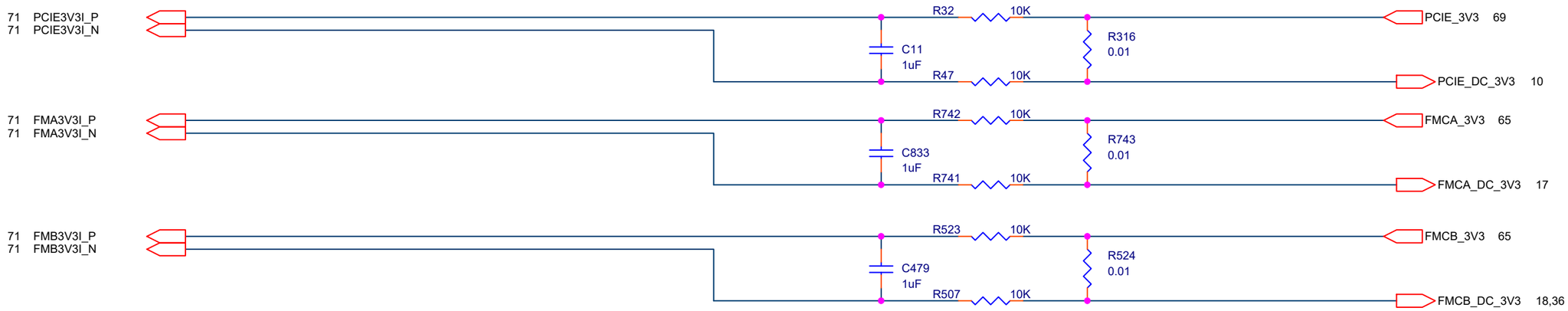
User DC Card 3.3V Current Sensors



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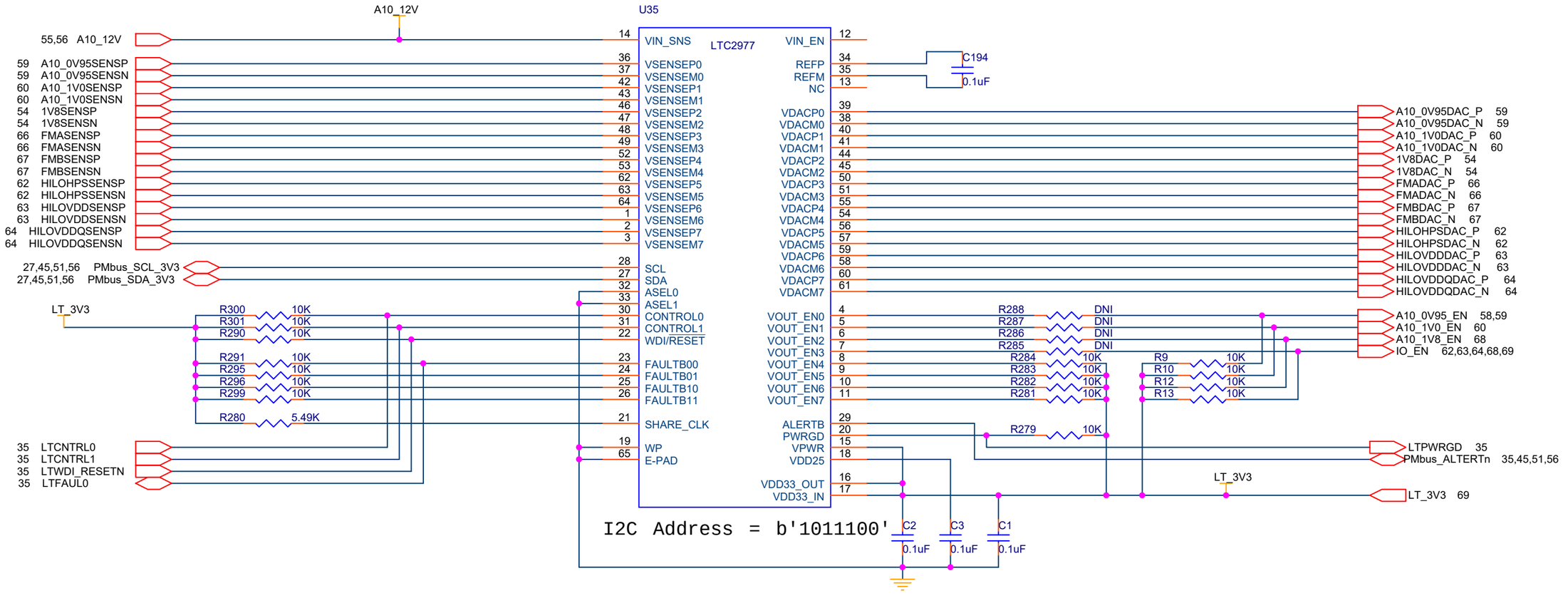
I2C Power ADC, DAC Controller



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Intel® Arria® 10 Power Inputs

77 A10_VCCAPLL
68 PLL_1V8

PLL_1V8

A10VCCPLLHPS 77
VCCIOREF_HPS 77
VCCIO_HPS 77
HPS_0V95 59
A10_VCCLSENSE 56
A10_GNDSENSE 56

U23Y

AE18 W19 W18 — VCCBAT VCCA_PLL VCCA_PLL
T24 T23 T20 T19 T17 T15 T14 AD25 AD24 AD20 AD16 AD15 AD14 — VCCP
N18 — VCCPLL_HPS
N16 M16 — VCCIOREF_HPS VCCIO_HPS
N17 P16 P18 R18 — VCCL_HPS VCCL_HPS VCCL_HPS VCCL_HPS
AA19 AA18 — VCCLSENSE GNDSENSE

PLL_1V8
1.8A
AD27 AH27 AM27 D27 H27 M27 T27 Y27 — VCCH_GXBL

60 A10_1V0
D29 D28 H29 H28 M29 M28 T29 T28 Y29 Y28 AD29 AD28 AH29 AH28 AM29 AM28 — VCCT_GXBL1J VCCT_GXBL1I VCCT_GXBL1H VCCT_GXBL1G VCCT_GXBL1F VCCT_GXBL1E VCCT_GXBL1D VCCT_GXBL1C

AP28 AP29 AK28 AK29 AF28 AF29 AB28 AB29 V28 V29 P28 P29 K28 K29 F28 F29 — VCCR_GXBL1C VCCR_GXBL1D VCCR_GXBL1E VCCR_GXBL1F VCCR_GXBL1G VCCR_GXBL1H VCCR_GXBL1I VCCR_GXBL1J

IO_1V8
VCCIO2A AK19 — IO_1V8 36,37,68
HILOHPS_VDD
VCCIO2A AM18 AP17 VCCIO2A AL21 VCCIO2I AP22 VCCIO2I AT21 VCCIO2I AK24 VCCIO2J AN25 VCCIO2J AR24 VCCIO2J E24 VCCIO2K H25 VCCIO2K K24 — HILOHPS_VDD 62
IO_1V8
VCCIO2K H20 VCCIO2L J22 VCCIO2L K19 VCCIO2L AK14 — FMCBVADJ 67
VCCIO3A AL11 VCCIO3A AM13 VCCIO3A AK9 — HILO_VDDQ 64
VCCIO3B AL6 VCCIO3B AM8 VCCIO3B AD7 VCCIO3C AG8 VCCIO3C AH5 VCCIO3C AA6 VCCIO3D AC5 VCCIO3D Y4 VCCIO3D R4
IO_1V8
VCCIO3E T6 VCCIO3E V5 VCCIO3E K4 — FMCAVADJ 66
VCCIO3F L6 VCCIO3F M8 VCCIO3F G8 VCCIO3G K9 VCCIO3G L11 VCCIO3G G13 VCCIO3H J12 VCCIO3H K14 VCCIO3H

U23Q

AF21 AF22 P21 P23 R12 R13 R14 R15 R16 R17 R20 R21 R22 R23 R25 T12 T13 T18 T22 T25 U12 U14 U19 U24 U25 U26 V12 V13 V14 V16 V17 V18 V19 V21 V22 V23 V24 W13 W14 W20 W21 W23 W24 W25 Y14 Y16 — VCC

VCC AA12 AA13 AA14 AA15 AA16 AA20 AA22 AA23 AA24 AA25 AB12 AB15 AB16 AB17 AB19 AB20 AB21 AB22 AB24 AB25 AC12 AC13 AC18 AC23 AC24 AC26 AD13 AD17 AD18 AD19 AD21 AD22 AD23 AE12 AE13 AE14 AE15 AE16 AE17 AE21 AE22 AE25 Y17 Y20 Y25 — VCC

A10_0V9 56

U22 U21 U20 U17 U16 U15 AC21 AC19 AC17 AC16 AC14 AB14 — VCCPT
AF19 AF18 — VCCPGM
Y12 Y13 Y18 Y21 Y22 Y23 — VCCERAM
D16 D15 M15 P13 T10 W11 Y11 AD11 AF13 AH16 P22 P24 AF23 AE23 AG19 — VREFP_ADC VREFN_ADC VREFB3HN0 VREFB3GN0 VREFB3FN0 VREFB3EN0 VREFB3DN0 VREFB3CN0 VREFB3BN0 VREFB3AN0 VREFB2LN0 VREFB2KN0 VREFB2JN0 VREFB2IN0 VREFB2AN0

A10SOC_1517

PLL_1V8
2A
IO_1V8
3A
58 0V95

VREFB2A VREFB2I VREFB2J VREFB2K VREFB2L VREFB3A VREFB3B VREFB3C VREFB3D

0.1uF 0.1uF 0.1uF 0.1uF
C719 C524 C554 C523

R519 240
R521 240
R520 240
R645 240
R646 DNI
R518 240

A10SOC_1517
IO_1V8
HILOHPS_VDD
IO_1V8
FMCBVADJ
HILO_VDDQ

R580 240
R591 240
R599 240

IO_1V8
R674
100K
D40
GND VOUT
GND
NC1 NC2 NC3 NC7 NC8
LT1389
C741
0.1uF

R672 240
R631 240
R619 240
R618 240
R600 240
R592 240
R581 240
R535 240
R644 240
R643 240
R537 240
R538 DNI
R536 DNI

VREFB3E VREFB3F VREFB3G VREFB3H

IO_1V8
FMCAVADJ
R616 240
R617 240
R630 240
R678 240

C720 C522 C521 C567 C566 C644 C675 C673 C711
0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF

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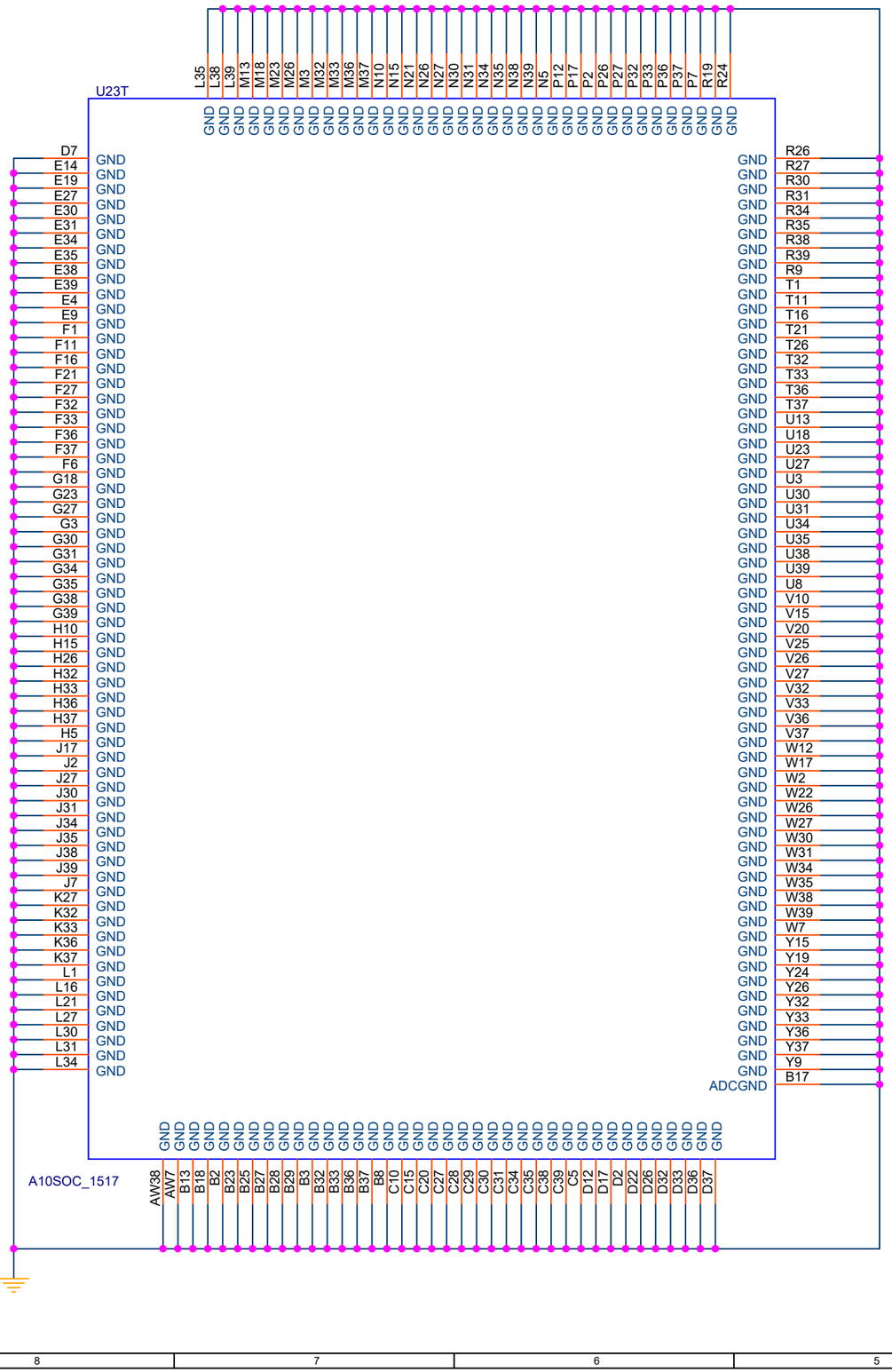
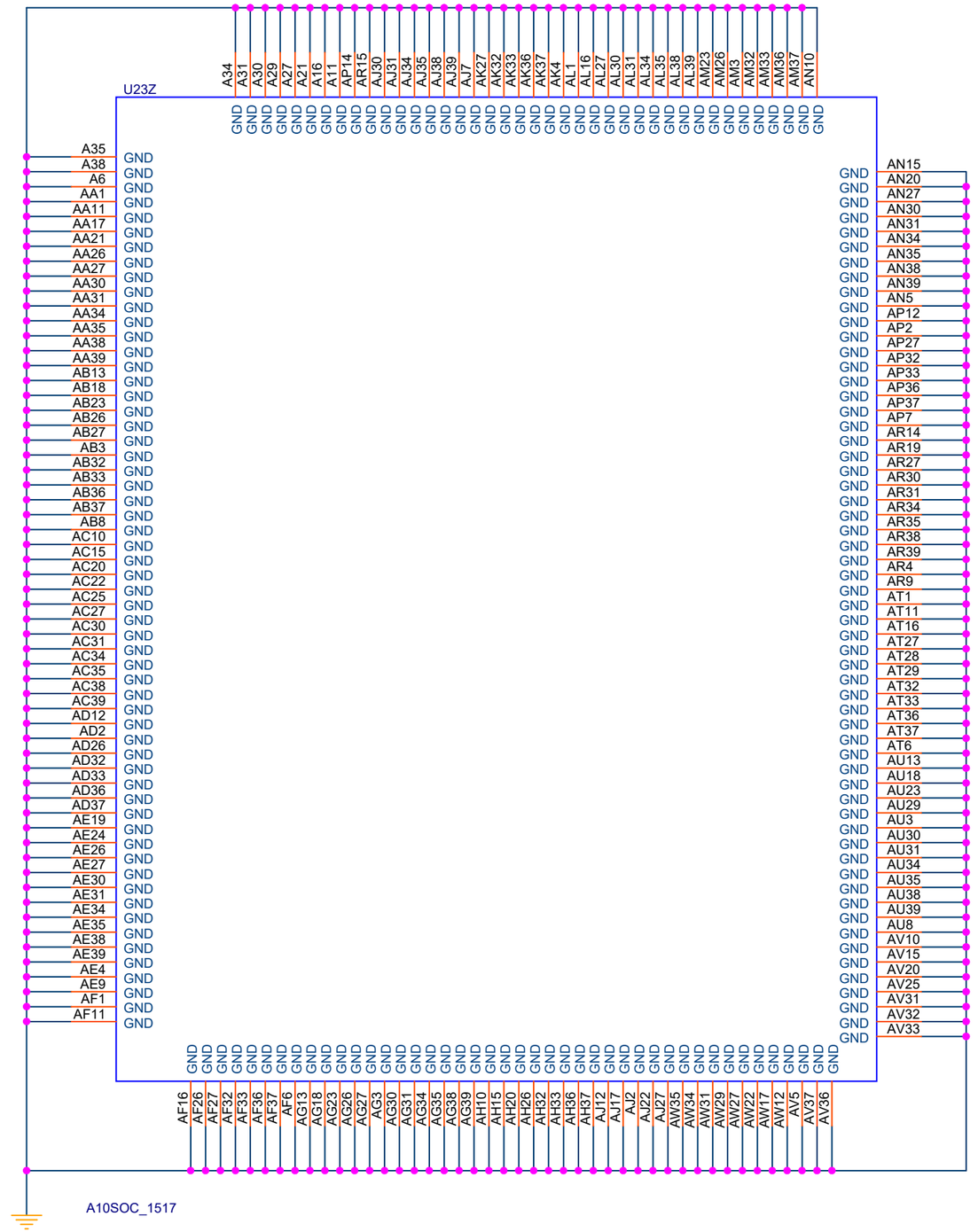
Intel® Arria® 10 Ground Connections





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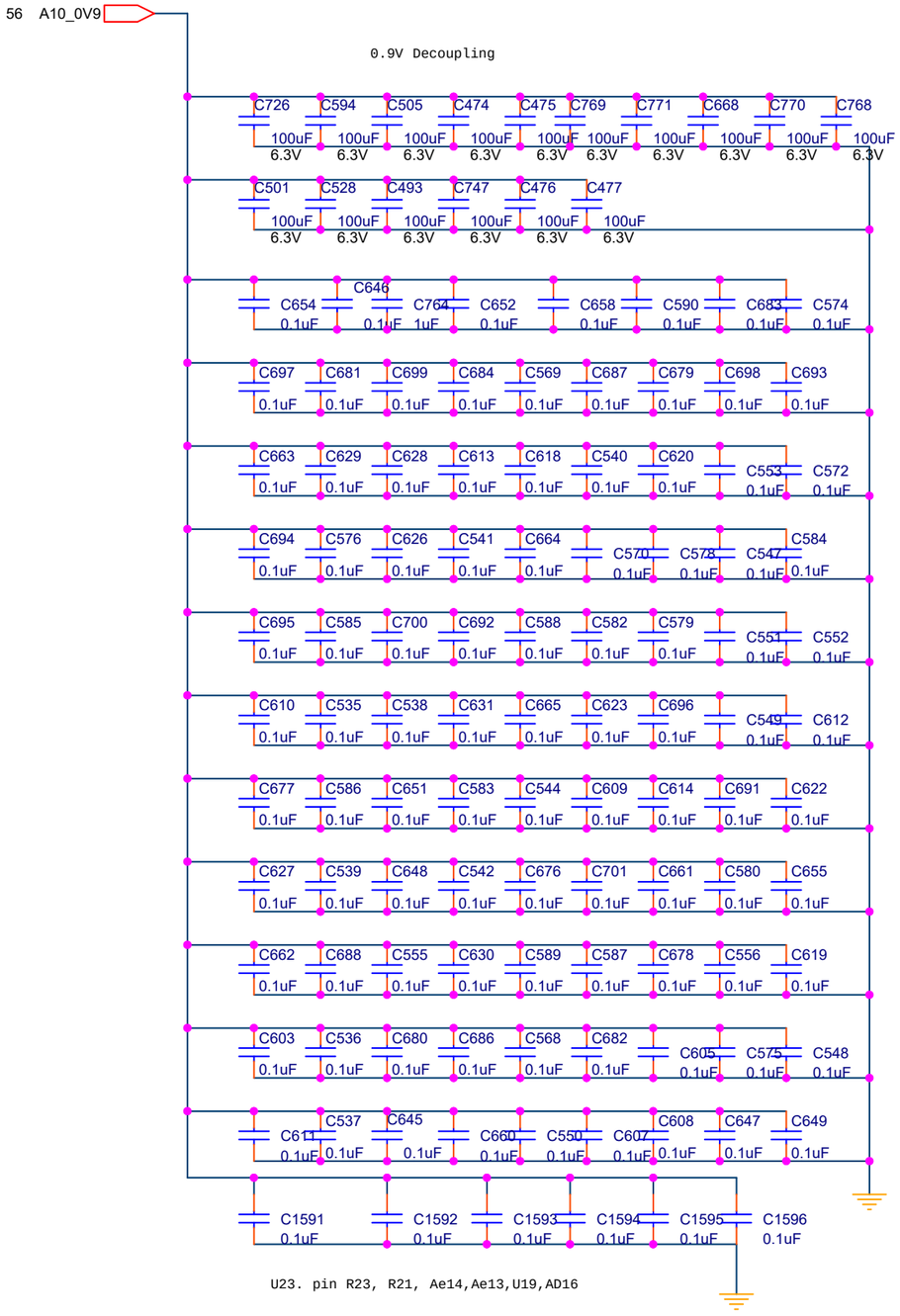
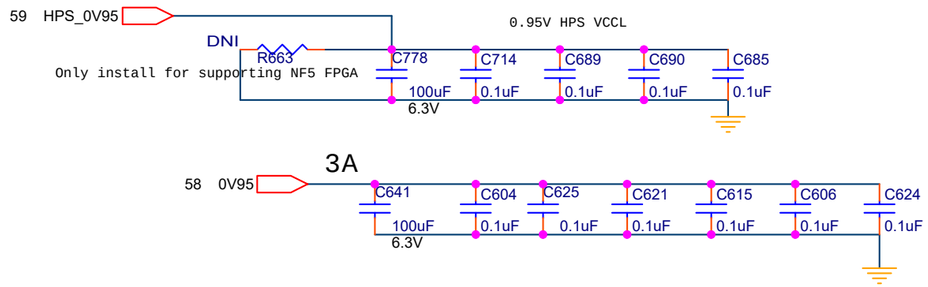
Reference Design Intel® Arria® 10 Core (VCC) Power Decoupling

(Based on Intel® Arria® 10 SoC Development Kit)



0.95V HPS is for boost mode



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Reference Design IO Power Decoupling

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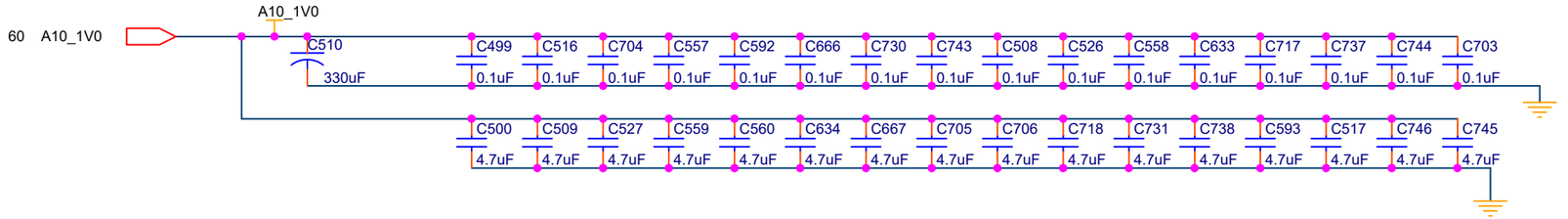

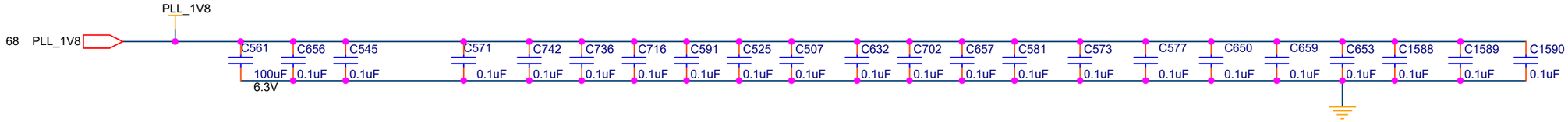

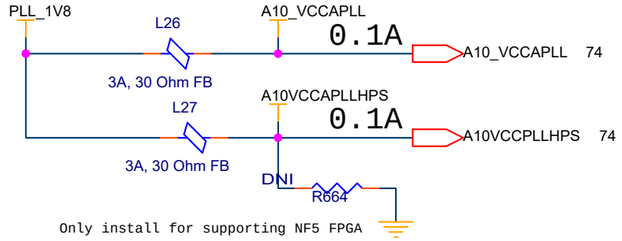

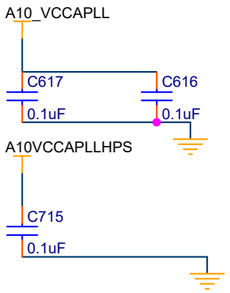

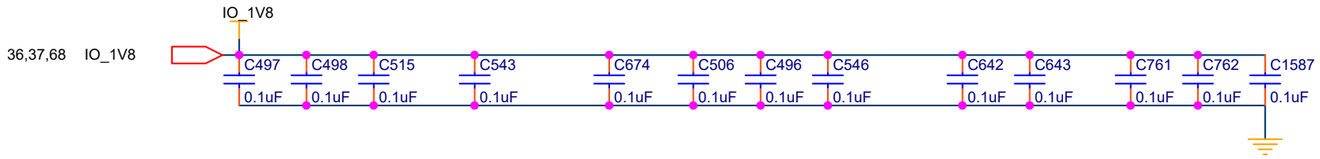

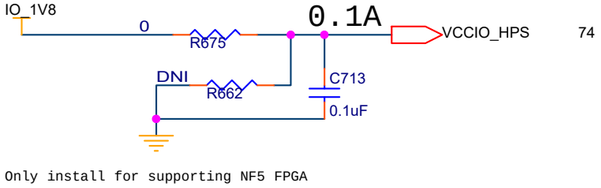

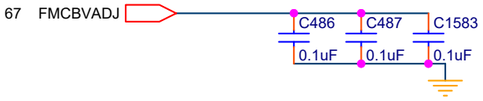

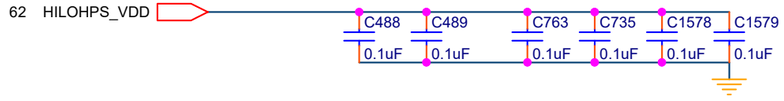

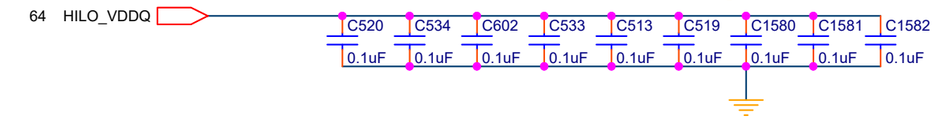

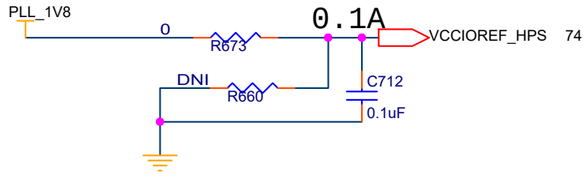

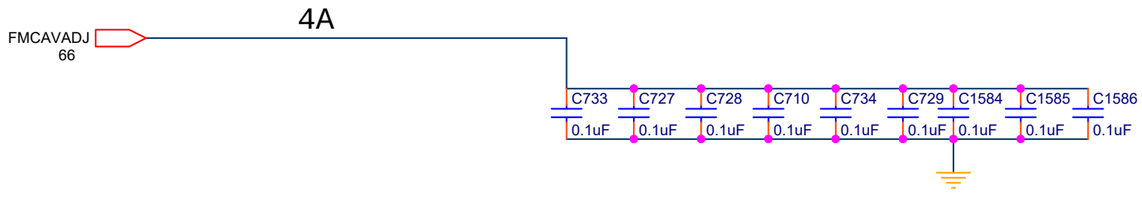

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